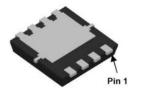
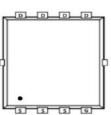
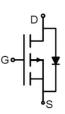


Main Product Characteristics:

V _{DSS}	-30V		
R _{DS} (on)	5.4mΩ (typ.)		
ID	-54A		







PDFN3x3-8L

Pin Assignments

Schematic Diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature



Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V ①	-54	
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V ①	-34	A
Ідм	Pulsed Drain Current ②	-216	
P _D @T _C = 25°C	Power Dissipation ③	33	W
V _{DS}	Drain-Source Voltage	-30	V
V _{GS}	Gate-to-Source Voltage	± 20	V
Eas	Single Pulse Avalanche Energy @ L=0.5mH	289	mJ
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C



Thermal Resistance

Symbol	Characterizes	Тур.	Max.	Units
Rejc	Junction-to-case ③	_	3.7	°C/W

Electrical Characterizes @TA=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source breakdown voltage	-30	_	_	V	V _{GS} = 0V, I _D = -250µA
Р	Static Drain-to-Source on-resistance		5.4	7	mΩ	V _{GS} = -10V,I _D = -20A
R _{DS(on)} Static Drain-te	Static Drain-to-Source on-resistance		8.7	11.6	1112	V _{GS} = -4.5V,I _D = -15A
$V_{GS(th)}$	Gate threshold voltage	-1	_	-2.5	V	$V_{DS} = V_{GS}, I_D = -250 \mu A$
I _{DSS}	Drain-to-Source leakage current		_	-1	μA	$V_{DS} = -30V, V_{GS} = 0V$
	Cata ta Sauraa fanward laakaga		_	100	~^	V _{GS} =20V
I _{GSS}	Gate-to-Source forward leakage		_	-100	nA	V _{GS} = -20V
Ciss	Input capacitance		3240	_		V _{GS} = 0V
Coss	Output capacitance		380	_	pF	V _{DS} = -15V
Crss	Reverse transfer capacitance		230	_		f = 1MHz
Qg	Total gate charge		60	_		I _D = -20A,
Q _{gs}	Gate-to-Source charge		7.5	_	nC	V _{DS} =-15V,
Q _{gd}	Gate-to-Drain("Miller") charge		15.5	_		V _{GS} = -10V
t _{d(on)}	Turn-on delay time		20	_		
t _r	Rise time	_	18	—		V_{GS} =-10V, V_{DS} =-15V,
t _{d(off)}	Turn-Off delay time	_	25	_	ns	$R_{GEN}=3\Omega, R_L=0.75\Omega$
t _f	Fall time	_	8	—		

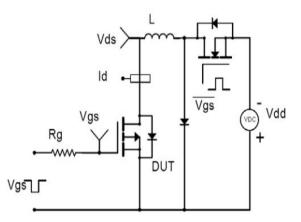
Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
1	Continuous Source Current			-54	^	MOSFET symbol ្ঢ
Is	(Body Diode)				showing the	
1	Pulsed Source Current			-216	^	integral reverse G⊶ 🕂 💆
Ism	(Body Diode)		210	A	p-n junction diode I_{s}	
V _{SD}	Diode Forward Voltage		_	-1.2	V	Is=-20A, V _{GS} =0V
t _{rr}	Reverse Recovery Time		15		ns	T _J = 25°C, I _F =-10A, di/dt =
Qrr	Reverse Recovery Charge	—	20	—	nC	100A/µs

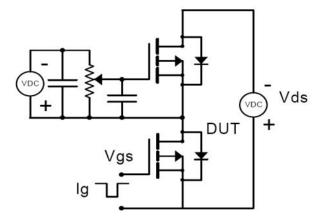


Test Circuits and Waveforms

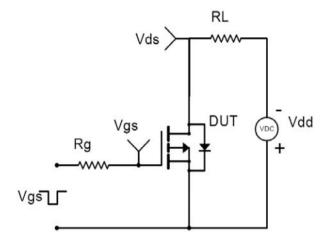
EAS Test Circuit:



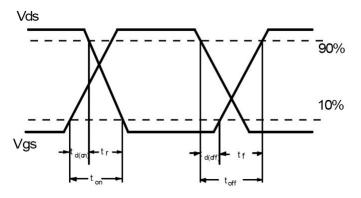
Gate Charge Test Circuit:



Switching Time Test Circuit:



Switching Waveforms:

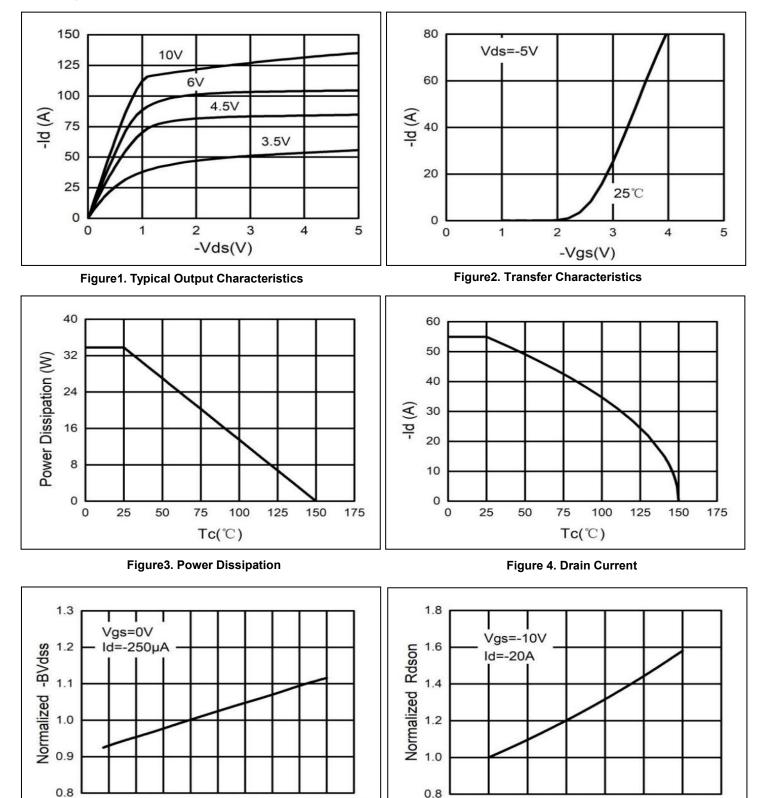


Notes:

- ①Calculated continuous current based on maximum allowable junction temperature.
- 2 Repetitive rating; pulse width limited by max. junction temperature.
- ③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.



Typical Electrical and Thermal Characteristics



Tj(℃)

50

25

0

-75 -50 -25

75 100 125 150 175



75

Figure6. RDS(ON) vs Junction Temperature

Tj(℃)

100

125

25

0

50

150

175



Typical Electrical and Thermal Characteristics

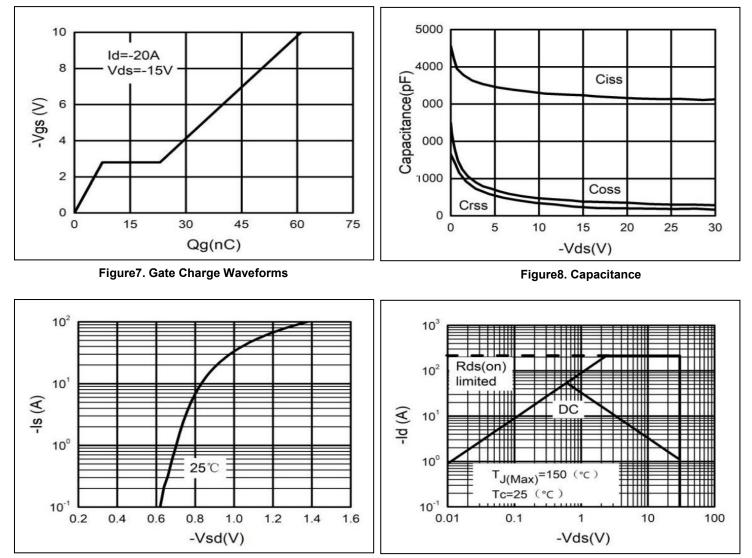
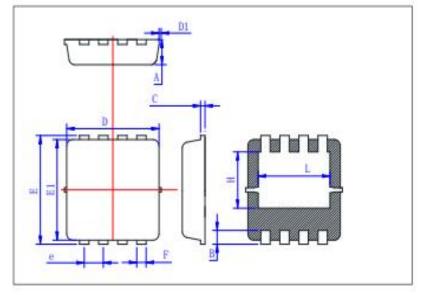


Figure9. Body-Diode Characteristics

Figure10. Maximum Safe Operating Area



Mechanical Data:



Symbol	Min	Тур	Max
A	0.725	0.775	0.825
В	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
DI			0.10
E	3.25	3.35	3.45
El	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.25	0.30	0.35
Н	1.63	1.73	1.83
L	2.35	2.45	2.55



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