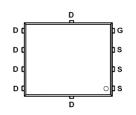
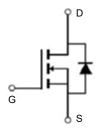


Main Product Characteristics:

V _{DSS}	60V
R _{DS} (on)	1.9mΩ (typ.)
I _D	160A







PDFN5x6-8L

Pin Assignments

Schematic Diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature



Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units		
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V ①	160			
I _D @ T _C = 100°C	@ T _C = 100°C Continuous Drain Current, V _{GS} @ 10V ①				
I _{DM}	Pulsed Drain Current ②	640			
P _D @T _C = 25°C	Power Dissipation ③	125	W		
V _{DS}	Drain-Source Voltage	60	V		
V _{GS}	Gate-to-Source Voltage	± 20	V		
E _{AS}	Single Pulse Avalanche Energy @ L=0.5mH	400	mJ		
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C		



Thermal Resistance

Symbol	Characterizes	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	_	1	°C /W
$R_{\theta JA}$	Junction-to-ambient (t \leq 10s) (4)	_	42	°C /W

Electrical Characterizes @T_A=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source breakdown voltage	60	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$
R _{DS(on)} St	Otatia Danie ta Carres an maiatarra	_	1.9	2.5	O	V _{GS} =10V,I _D = 20A
	Static Drain-to-Source on-resistance	_	2.5	3.3	mΩ	V _{GS} =4.5V,I _D = 15A
V _{GS(th)}	Gate threshold voltage	1	_	2.5	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
I _{DSS}	Drain-to-Source leakage current	_	_	1	μΑ	$V_{DS} = 60V, V_{GS} = 0V$
	Cata ta Caura famuard la disasa	_	_	100		V _{GS} =20V
I _{GSS}	Gate-to-Source forward leakage	_	_	-100	nA	V _{GS} = -20V
C _{iss}	Input capacitance	_	5350	_		V _{GS} = 0V
Coss	Output capacitance	_	2150	_	pF	V _{DS} = 25V
C _{rss}	Reverse transfer capacitance	_	105	_		f = 1MHz
Qg	Total gate charge	_	100	_		I _D = 30A,
Q _{gs}	Gate-to-Source charge	_	15	_	nC $V_{DS}=30V$,	V _{DS} =30V,
Q_{gd}	Gate-to-Drain("Miller") charge	_	20	_		V _{GS} = 10V
t _{d(on)}	Turn-on delay time	_	15	_		
t _r	Rise time	_	38	_		V_{GS} =10V, V_{DD} =30V,
t _{d(off)}	Turn-Off delay time	_	75	_	ns	$R_{GEN}=3\Omega, I_D=30A$
t _f	Fall time	_	95	_		

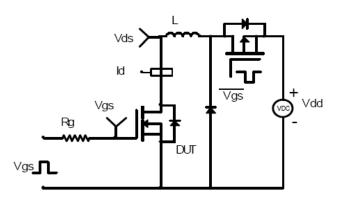
Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current	_	_	160	А	MOSFET symbol
	(Body Diode)					showing the
I _{SM}	Pulsed Source Current	_	_	640	А	integral reverse
	(Body Diode)					p-n junction diode.
V _{SD}	Diode Forward Voltage	_	_	1.2	V	I _S =30A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	_	54.7	_	ns	$T_J = 25^{\circ}C, I_F = 30A, di/dt =$
Q _{rr}	Reverse Recovery Charge	_	60	_	nC	100A/µs

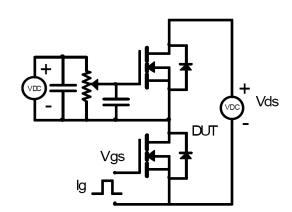


Test Circuits and Waveforms

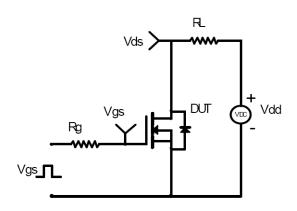
EAS Test Circuit:



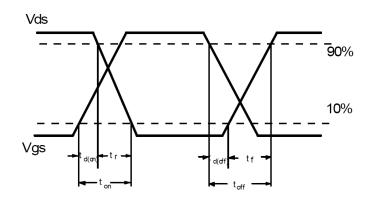
Gate Charge Test Circuit:



Switching Time Test Circuit:



Switching Waveforms:



Version: Preliminary

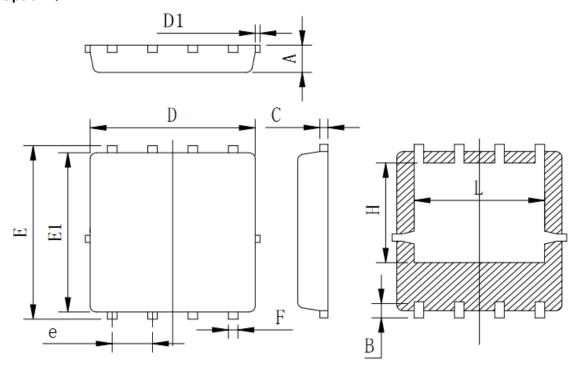
Notes:

- ①Calculated continuous current based on maximum allowable junction temperature.
- (2) Repetitive rating; pulse width limited by max. junction temperature.
- (3) The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- 4The value of $R_{\textcircled{9JA}}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C



Mechanical Data:

Option1:

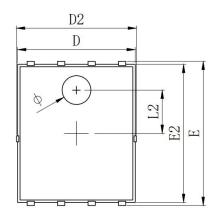


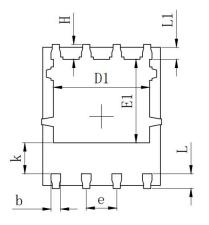
Symbol	Min	Тур	Max
A	0.90	0.95	1.00
В	B 0.48 0.58		0.68
С	0.20	0.254	0.30
D	5.00	5.20	5.40
D1			0.15
Е	5.90	6.05	6.20
El	5.40	5.55	5.70
e	1.22	1.27	1.32
F	0.25	0.30	0.35
Н	3.27	3.47	3.67
L	3.80	4.00	4.20

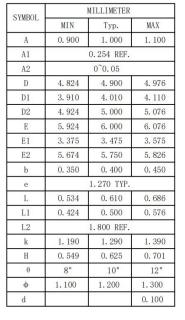


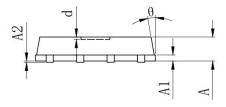


Option2:













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