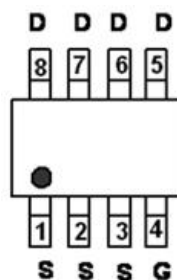


Main Product Characteristics:

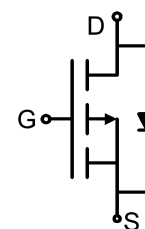
V_{DSS}	-40V
$R_{DS(on)}$	11.6m Ω (typ.)
I_D	-13A ①



SOP-8



Pin Assignment



Schematic Diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current ①	-13	A
I_{DM}	Pulsed Drain Current ②	-52	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ③	4	W
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.5mH	128	mJ
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
R _{θJA}	Junction-to-ambient (t ≤ 10s) ④	—	31.2	°C/W

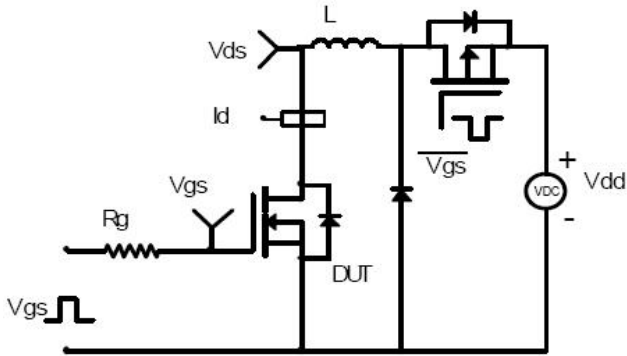
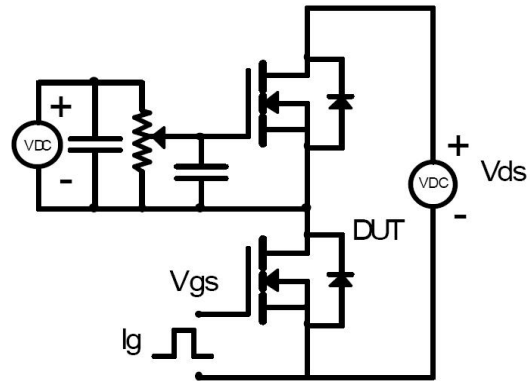
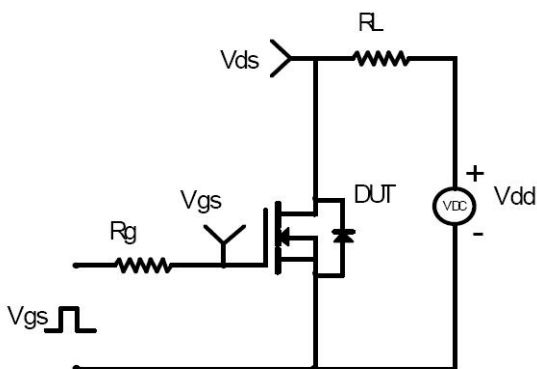
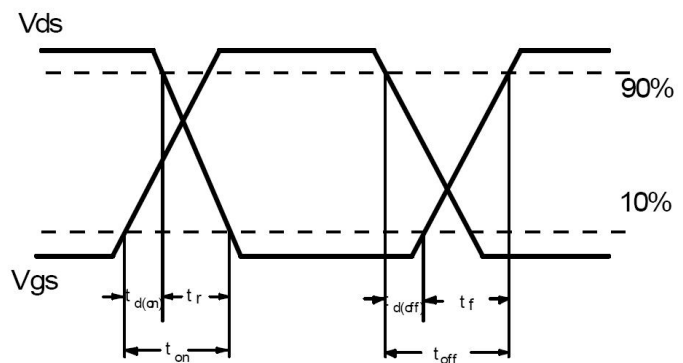
Electrical Characterizes @T_A=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source breakdown voltage	-40	—	—	V	V _{GS} = 0V, I _D = -250μA
R _{DS(on)}	Static Drain-to-Source on-resistance	—	11.6	15	mΩ	V _{GS} =-10V, I _D = -10A
		—	15	22	mΩ	V _{GS} =-4.5V, I _D = -8A
V _{GS(th)}	Gate threshold voltage	-1	—	-2.5	V	V _{DS} = V _{GS} , I _D = -250μA
I _{DSS}	Drain-to-Source leakage current	—	—	-1	μA	V _{DS} = -40V, V _{GS} = 0V
I _{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V _{GS} = 20V
		—	—	-100		V _{GS} = -20V
Q _g	Total gate charge	—	20	—	nC	I _D = -10A, V _{DS} =-32V, V _{GS} = -4.5V
Q _{gs}	Gate-to-Source charge	—	8	—		
Q _{gd}	Gate-to-Drain("Miller") charge	—	8.5	—		
t _{d(on)}	Turn-on delay time	—	21.8	—	ns	V _{GS} =-10V, V _{DS} =-20V, R _{GEN} =3Ω, I _D =-20A
t _r	Rise time	—	87.2	—		
t _{d(off)}	Turn-Off delay time	—	49.5	—		
t _f	Fall time	—	54.8	—		
C _{iss}	Input capacitance	—	3860	—	pF	V _{GS} = 0V V _{DS} = -25V f = 1MHz
C _{oss}	Output capacitance	—	250	—		
C _{riss}	Reverse transfer capacitance	—	240	—		

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode) ①	—	—	-13	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-52	A	
V _{SD}	Diode Forward Voltage	—	—	-1.2	V	

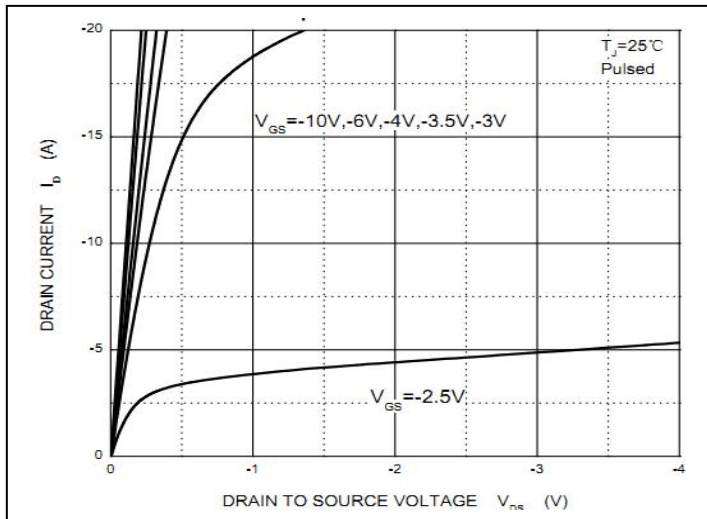
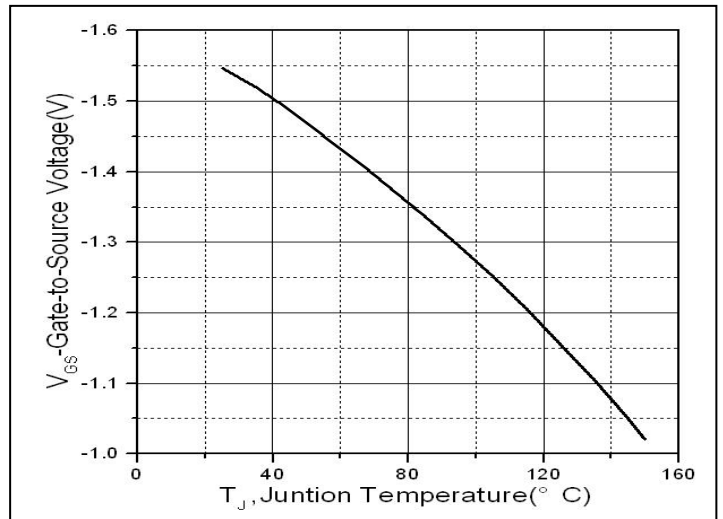
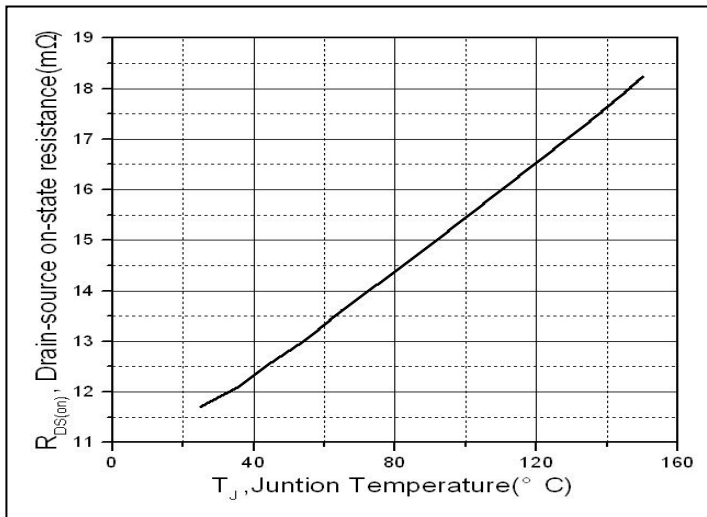
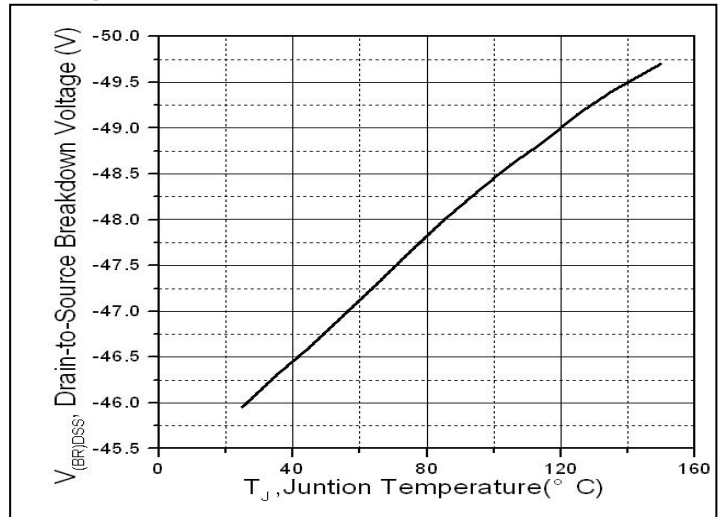
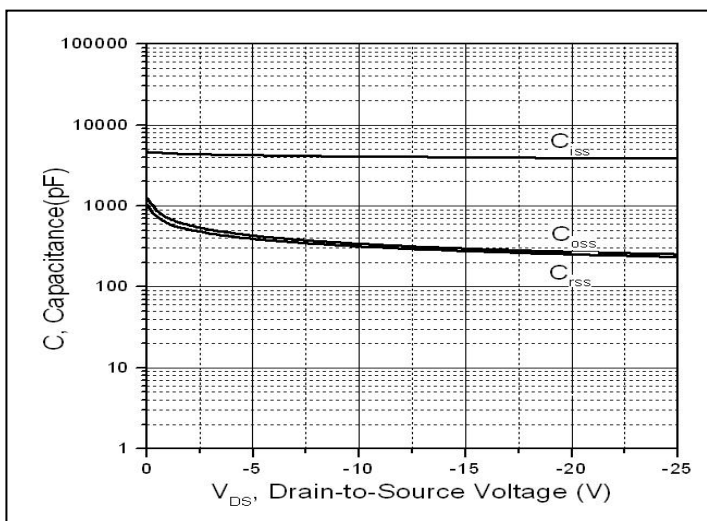
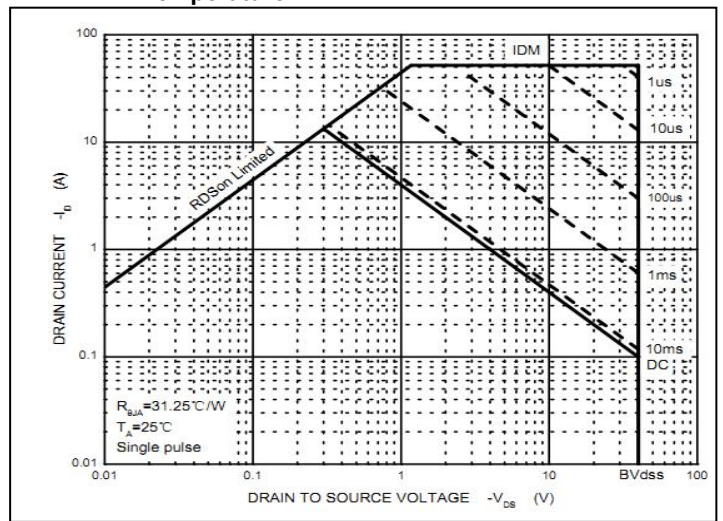
Test Circuits and Waveforms

EAS Test Circuit:

Gate Charge Test Circuit:

Switching Time Test Circuit:

Switching Waveforms:


Notes:

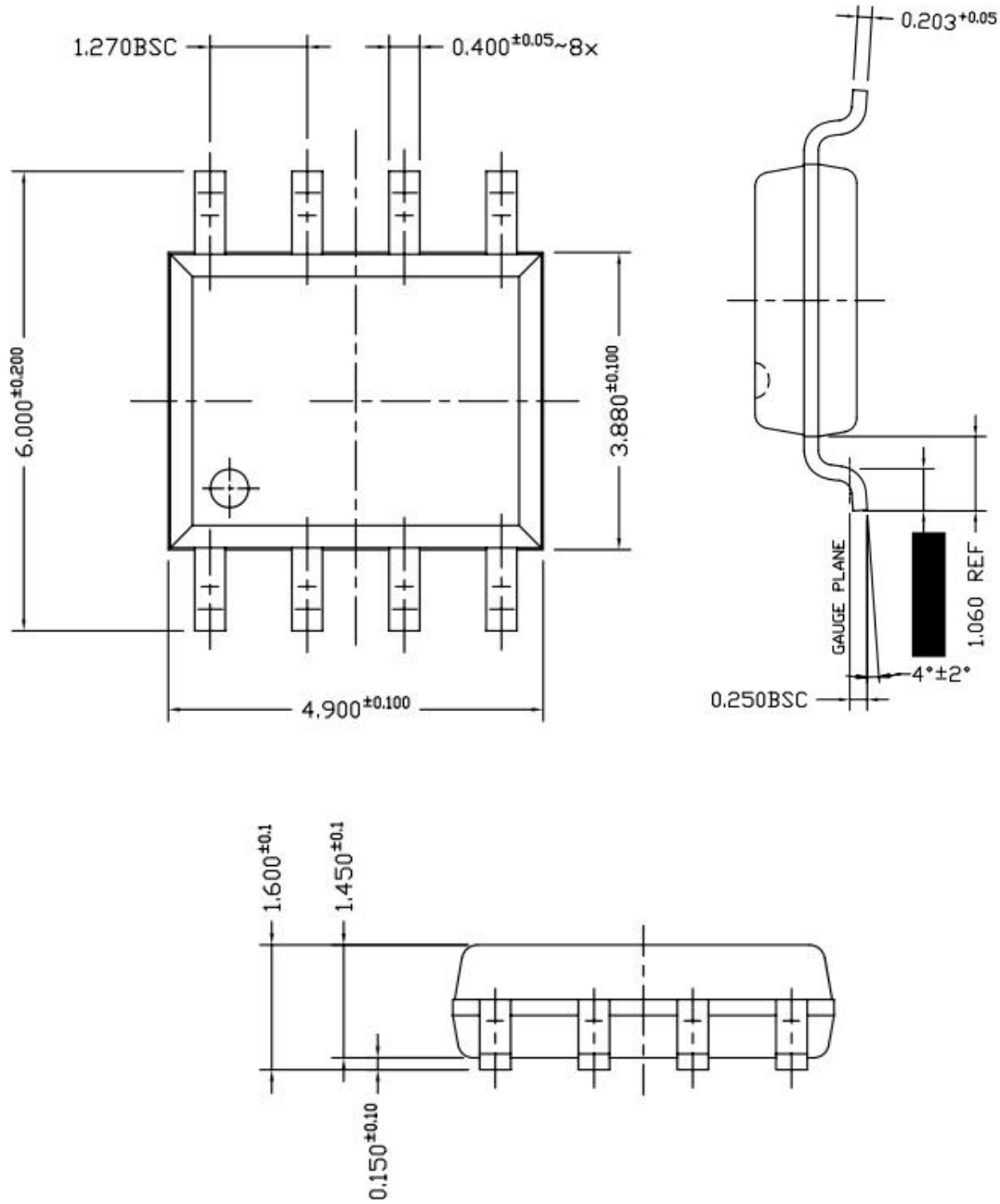
- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical Electrical and Thermal Characteristics


Figure 1. Typical Output Characteristics

Figure 2. Normalized $V_{GS(th)}$ vs. Junction Temperature

Figure 3. Normalized On-Resistance vs. Junction Temperature

Figure 4. Drain-to-Source Breakdown Voltage vs. Junction Temperature

Figure 5. Capacitance Characteristics

Figure 6. Safe Operation Area

Mechanical Data:

SOP-8 Package Outline (Unit:mm)



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