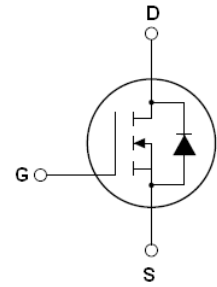


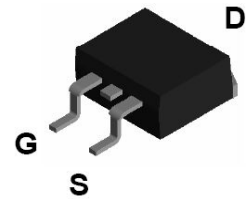
**Features:**

- Advanced trench process technology
- Ultra low  $R_{ds(on)}$
- High avalanche energy, 100% test
- Fully characterized avalanche voltage and current

**$I_D = 60A$**   
 **$BV = 110V$**   
 **$R_{ds(on)} = 20m\Omega$  (Typ.)**


**Description:**

The SSF1122D is a new generation of middle voltage and high current N-Channel enhancement mode trench power MOSFET. This new technology increases the device reliability and electrical parameter repeatability. SSF1122D is assembled in high reliability and qualified assembly house.



SSF1122D TOP View (DPAK)

**Application:**

- Power switching application

**Absolute Maximum Ratings**

|                           | Parameter  | Max.        | Units |
|---------------------------|--|-------------|-------|
| $I_D @ T_c = 25^\circ C$  | Continuous drain current, $V_{GS} @ 10V$         | 60          | A     |
| $I_D @ T_c = 100^\circ C$ | Continuous drain current, $V_{GS} @ 10V$         | 50          |       |
| $I_{DM}$                  | Pulsed drain current ①                           | 240         |       |
| $P_D @ T_c = 25^\circ C$  | Power dissipation                                | 143         | W     |
|                           | Linear derating factor                           | 2.0         | W/°C  |
| $V_{GS}$                  | Gate-to-Source voltage                           | $\pm 20$    | V     |
| $E_{AS}$                  | Single pulse avalanche energy ②                  | 240         | mJ    |
| $E_{AR}$                  | Repetitive avalanche energy                      | TBD         |       |
| $T_J$<br>$T_{STG}$        | Operating Junction and Storage Temperature Range | -55 to +175 | °C    |

**Thermal Resistance**

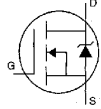
|                 | Parameter           | Min. | Typ. | Max. | Units |
|-----------------|---------------------|------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-case    | —    | 1.05 | —    | °C/W  |
| $R_{\theta JA}$ | Junction-to-ambient | —    | —    | 62   |       |

**Electrical Characteristics @  $T_J = 25^\circ C$  (unless otherwise specified)**

|              | Parameter                            | Min. | Typ. | Max. | Units      | Test Conditions                                 |
|--------------|--------------------------------------|------|------|------|------------|---|
| $BV_{DSS}$   | Drain-to-Source breakdown voltage    | 110  | —    | —    | V          | $V_{GS} = 0V, I_D = 250\mu A$                   |
| $R_{DS(on)}$ | Static Drain-to-Source on-resistance | —    | 20   | 22   | m $\Omega$ | $V_{GS} = 10V, I_D = 30A$                       |
| $V_{GS(th)}$ | Gate threshold voltage               | 2.0  | 3.0  | 4.0  | V          | $V_{DS} = V_{GS}, I_D = 250\mu A$               |
| $g_{fs}$     | Forward transconductance             | —    | 58   | —    | S          | $V_{DS} = 5V, I_D = 30A$                        |
| $I_{DSS}$    | Drain-to-Source leakage current      | —    | —    | 1    | $\mu A$    | $V_{DS} = 110V, V_{GS} = 0V$                    |
|              |                                      | —    | —    | 10   |            | $V_{DS} = 110V, V_{GS} = 0V, T_J = 150^\circ C$ |

|              |                                |   |      |      |    |                        |
|--------------|--------------------------------|---|------|------|----|------------------------|
| $I_{GSS}$    | Gate-to-Source forward leakage | — | —    | 100  | nA | $V_{GS}=20V$           |
|              | Gate-to-Source reverse leakage | — | —    | -100 |    | $V_{GS}=-20V$          |
| $Q_g$        | Total gate charge              | — | 90   | —    | nC | $I_D=30A$              |
| $Q_{gs}$     | Gate-to-Source charge          | — | 14   | —    |    | $V_{DD}=30V$           |
| $Q_{gd}$     | Gate-to-Drain("Miller") charge | — | 24   | —    |    | $V_{GS}=10V$           |
| $t_{d(on)}$  | Turn-on delay time             | — | 18.2 | —    | nS | $V_{DD}=30V$           |
| $t_r$        | Rise time                      | — | 15.6 | —    |    | $I_D=2A, R_L=15\Omega$ |
| $t_{d(off)}$ | Turn-Off delay time            | — | 70.5 | —    |    | $R_G=2.5\Omega$        |
| $t_f$        | Fall time                      | — | 13.8 | —    |    | $V_{GS}=10V$           |
| $C_{iss}$    | Input capacitance              | — | 3150 | —    | pF | $V_{GS}=0V$            |
| $C_{oss}$    | Output capacitance             | — | 300  | —    |    | $V_{DS}=25V$           |
| $C_{rss}$    | Reverse transfer capacitance   | — | 240  | —    |    | $f=1.0MHz$             |

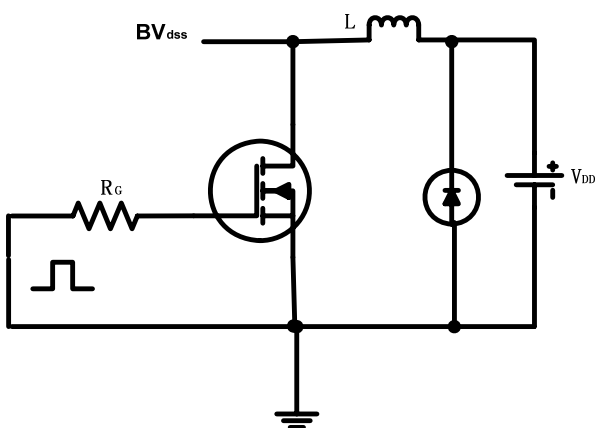
### Source-Drain Ratings and Characteristics

|          | Parameter                                 | Min.  | Typ. | Max. | Units | Test Conditions   |
|----------|---|---|------|------|-------|---|
| $I_S$    | Continuous Source Current<br>(Body Diode) | —   | —    | 60   | A     | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current<br>(Body Diode) ①   | —   | —    | 240  |       |   |
| $V_{SD}$ | Diode Forward Voltage                     | —   | —    | 1.3  | V     | $T_J=25C, I_S=30A, V_{GS}=0V$ ③   |
| $t_{rr}$ | Reverse Recovery Time                     | —   | 57   | —    | nS    | $T_J=25C, I_F=60A$  |
| $Q_{rr}$ | Reverse Recovery Charge                   | —   | 107  | —    | nC    | $di/dt=100A/\mu s$ ③  |
| $t_{on}$ | Forward Turn-on Time                      | Intrinsic turn-on time is negligible (turn-on is dominated by $L_s + L_D$ ) |      |      |       |   |

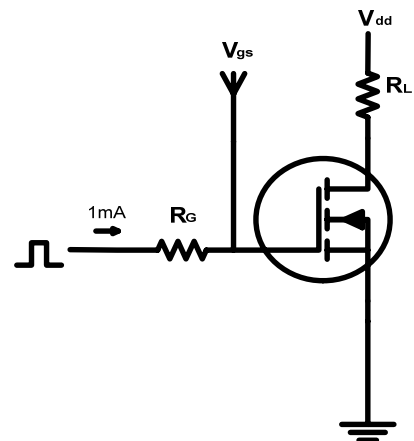
#### Notes:

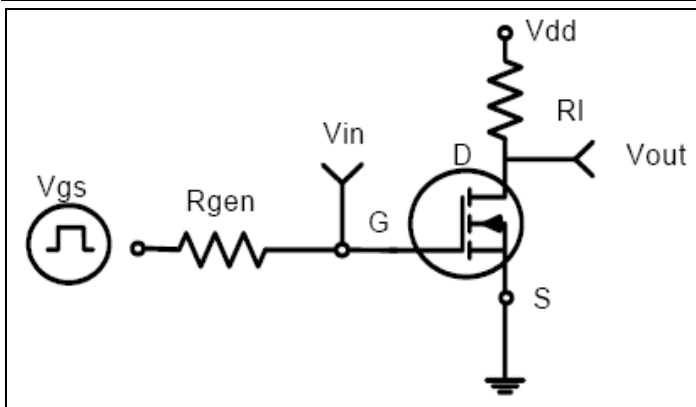
- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Test condition:  $L = 0.3mH, I_D = 40A, V_{DD} = 50V$
- ③ Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 1.5\%$ ;  $R_G = 25\Omega$  Starting  $T_J = 25^\circ C$

**EAS test circuit**

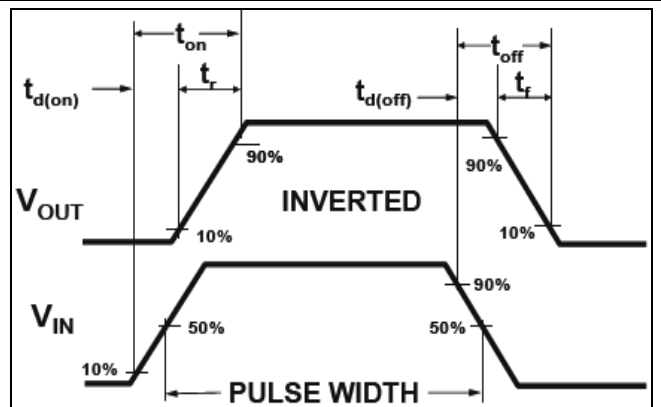


**Gate charge test circuit**

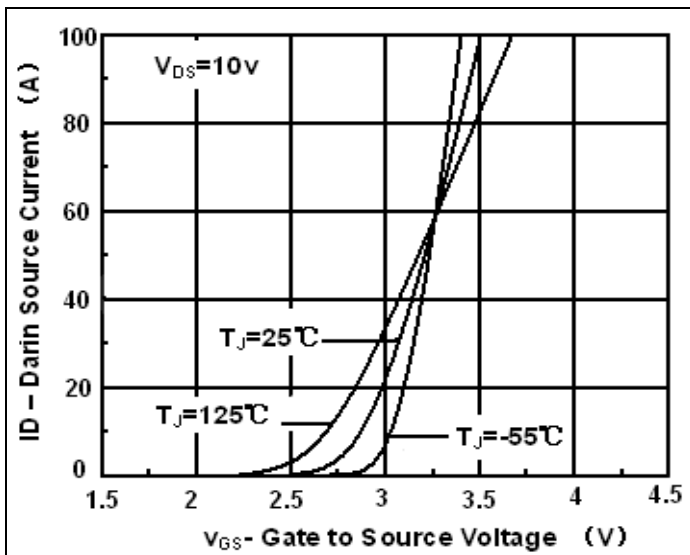




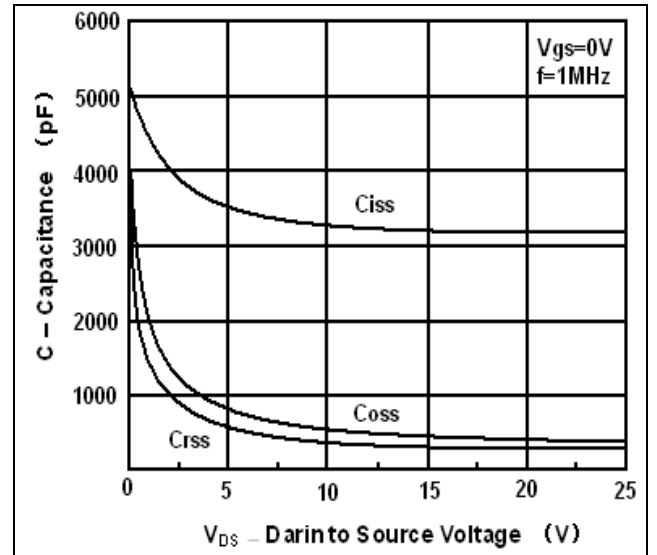
Switch Time Test Circuit:



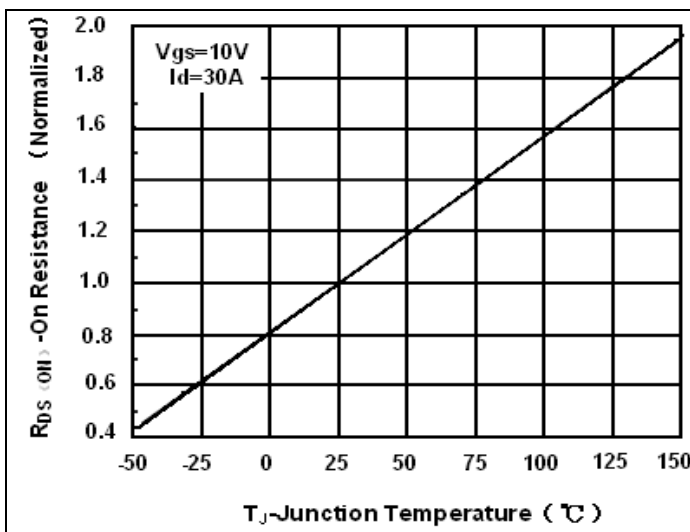
Switch Waveforms:



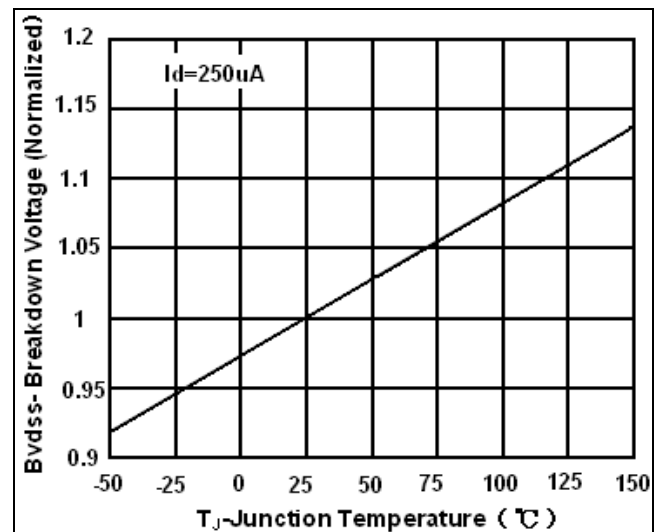
Transfer Characteristic



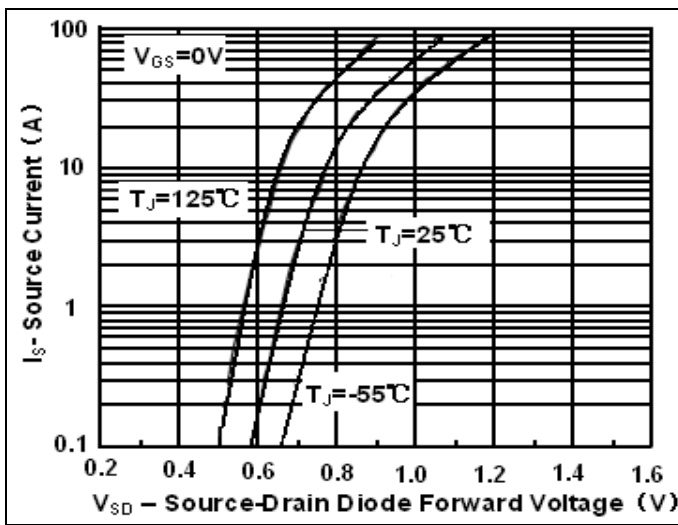
Capacitance:



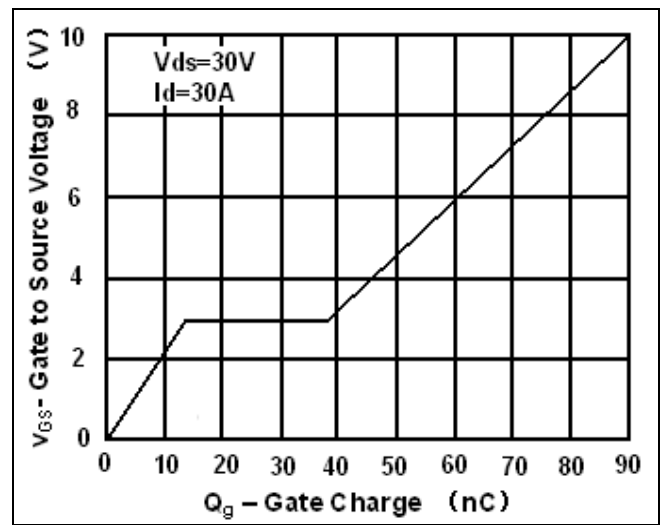
On Resistance vs. Junction Temperature



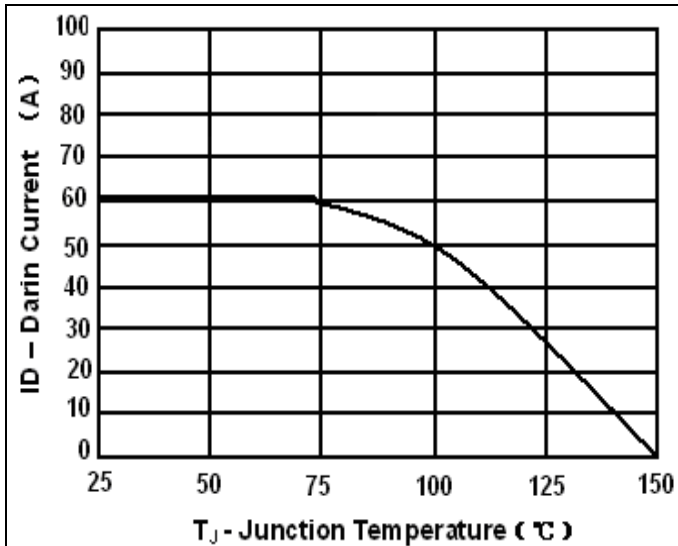
Breakdown Voltage vs. Junction Temperature



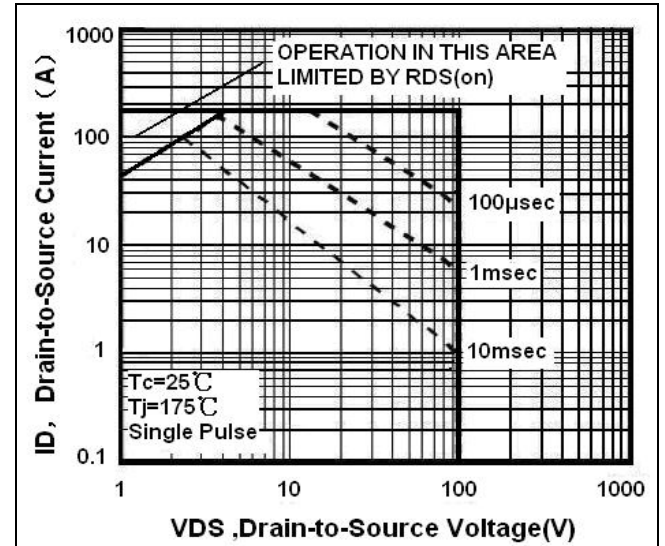
Source-Drain Diode Forward Voltage



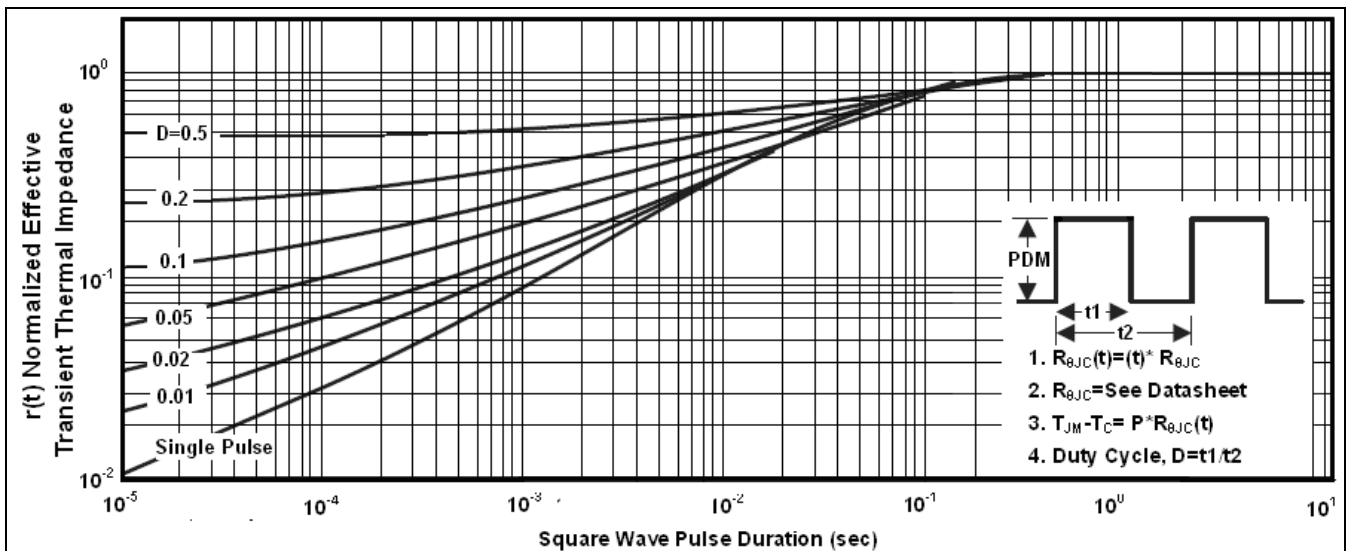
Gate Charge



Max Drain Current vs. Junction Temperature

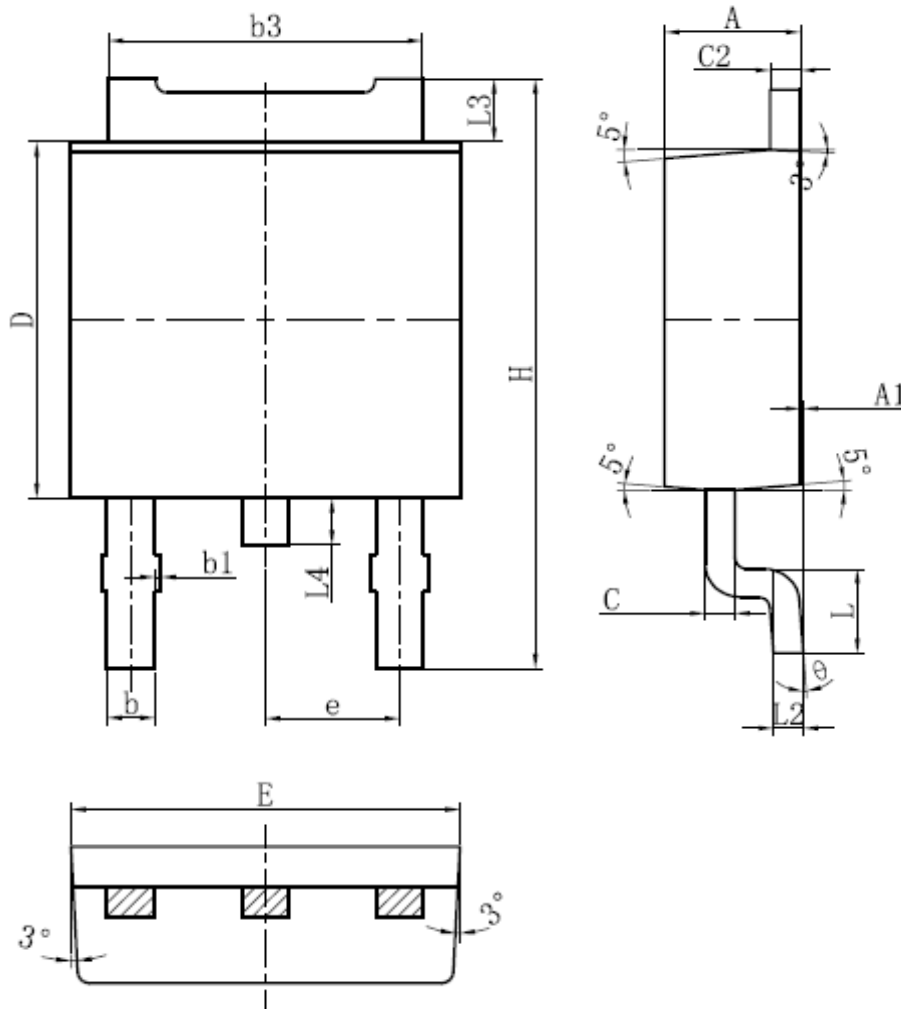


Safe Operation Area



Transient Thermal Impedance Curve

## DPAK MECHANICAL DATA:



| Symbol   | Mln.  | Normal  | Max.  |
|----------|-------|---------|-------|
| E        | 6.55  | 6.6     | 6.65  |
| L        | 1.40  | 1.5     | 1.60  |
| L2       | -     | 0.51BSC | -     |
| L3       | 0.93  | 1.08    | 1.23  |
| L4       | 0.7   | 0.8     | 0.9   |
| D        | 6.05  | 6.1     | 6.15  |
| H        | 9.9   | 10.1    | 10.3  |
| b        | 0.763 | 0.813   | 0.863 |
| b1       | 0     | -       | 0.1   |
| b3       | 5.28  | 5.33    | 5.38  |
| e        | 2.23  | 2.28    | 2.33  |
| A        | 2.25  | 2.3     | 2.35  |
| A1       | 0     | 0.05    | 0.10  |
| C        | 0.498 | 0.508   | 0.518 |
| C2       | 0.498 | 0.508   | 0.518 |
| $\theta$ | 0     | -       | 8°    |

### NOTE:

- 1.Package body size exclude flash and gate burrs.
- 2.Dimension L is measured in gage plane.
- 3.Tolerance 0.10mm unless otherwise specified.
- 4.Controlling dimension is millimeter. Converted inch dimension are not necessarily exact.