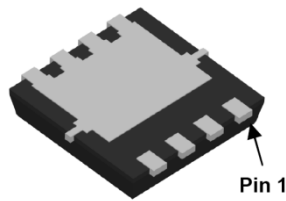
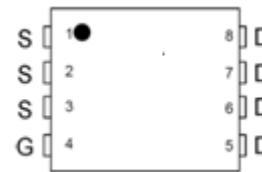
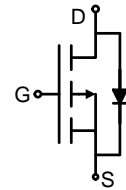


Main Product Characteristics:

V_{DSS}	-20V
$R_{DS(on)}$	3.6m Ω (typ.)
I_D	-50A


DFN3.3x3.3
Bottom view

Pin Assignment

Schematic Diagram
Features and Benefits:

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V ①	-50	A
I_{DM}	Pulsed Drain Current ②	-200	
P_D @TC = 25°C	Power Dissipation ③	83	W
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.1mH ②	80	mJ
I_{AR}	Avalanche Current @ L=0.1mH ②	40	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

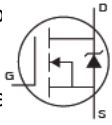
Thermal Resistance

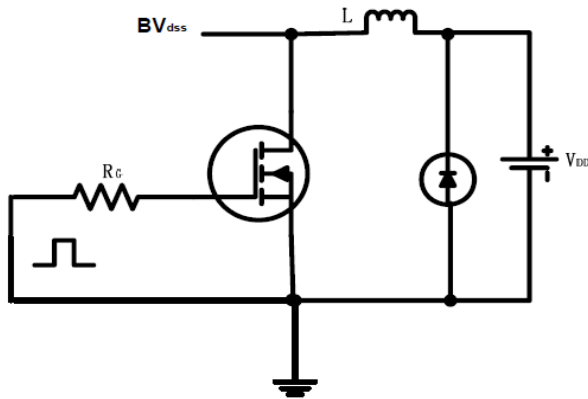
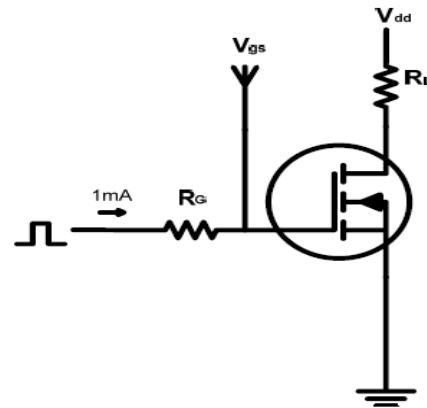
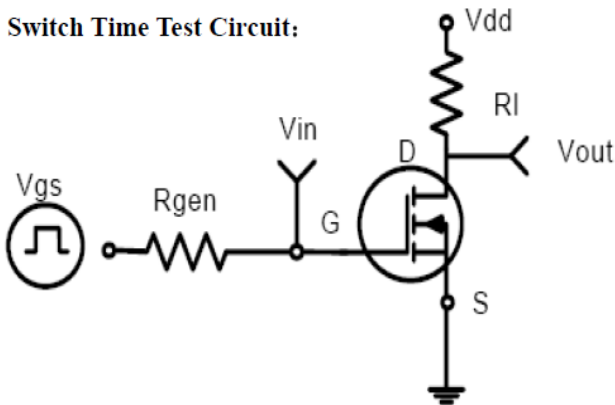
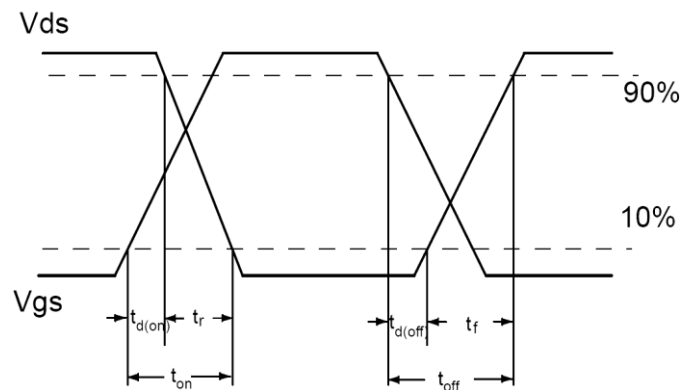
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	1.5	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	20	$^{\circ}C/W$

Electrical Characterizes @ $T_A=25^{\circ}C$ unless otherwise specified

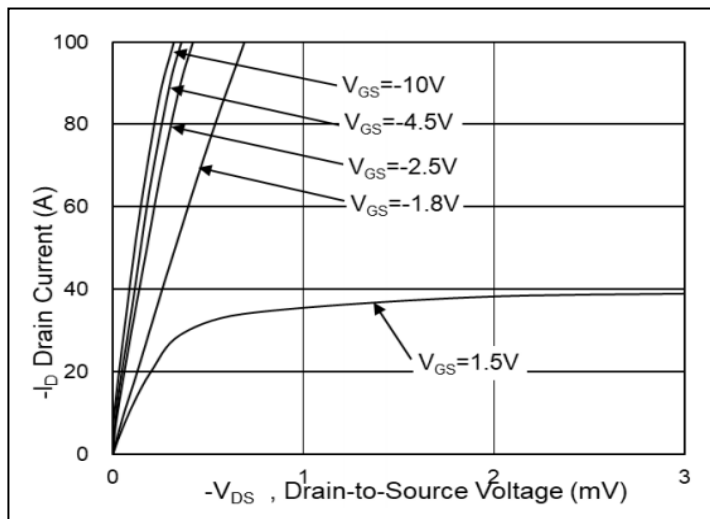
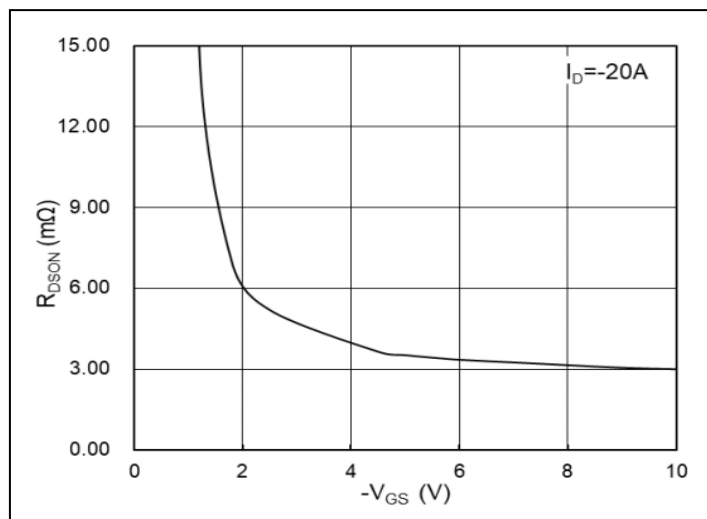
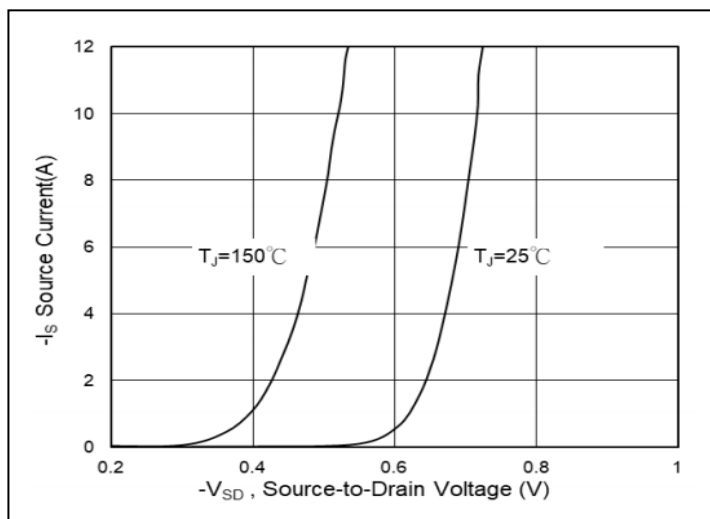
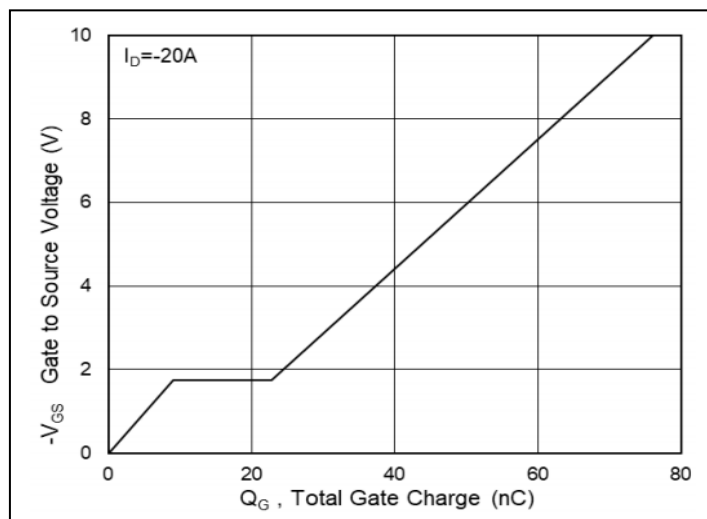
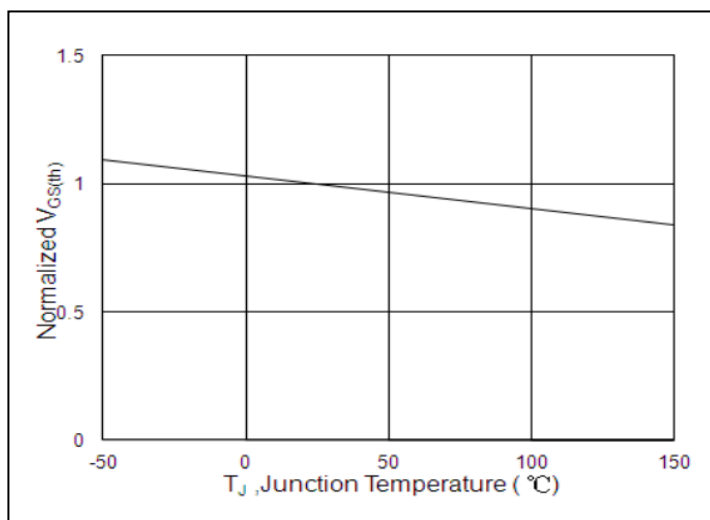
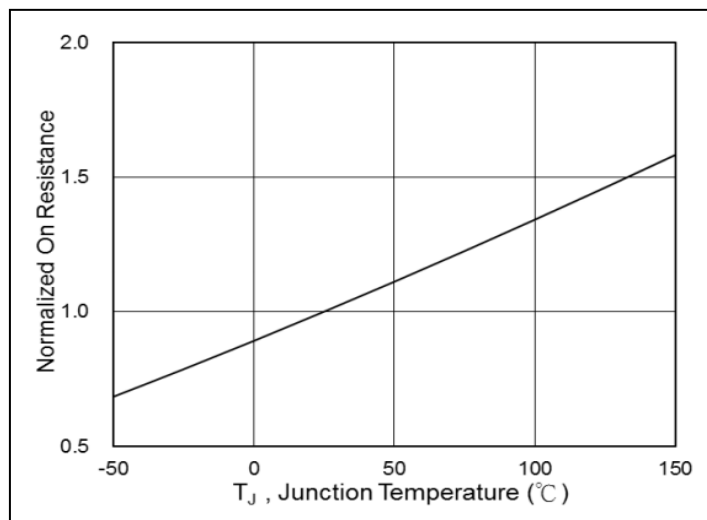
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	3.6	5	m Ω	$V_{GS}=-4.5V, I_D = -20A$
		—	4.7	6.5		$V_{GS}=-2.5V, I_D = -20A$
		—	6.4	8.5		$V_{GS}=-1.8V, I_D = -20A$
$V_{GS(th)}$	Gate threshold voltage	-0.35	—	-1	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
I_{DSS}	Drain-to-Source leakage current	—	—	-1	μA	$V_{DS} = -16V, V_{GS} = 0V$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 12V$
		—	—	-100		$V_{GS} = -12V$
Q_g	Total gate charge	—	75	—	nC	$I_D = -20A,$ $V_{DS} = -15V,$ $V_{GS} = -10V$
Q_{gs}	Gate-to-Source charge	—	10	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	14	—		
$t_{d(on)}$	Turn-on delay time	—	12	—	ns	$V_{GS} = -10V, V_{DS} = -15V,$ $I_D = -20A, R_{GEN} = 3\Omega$
t_r	Rise time	—	11	—		
$t_{d(off)}$	Turn-Off delay time	—	55	—		
t_f	Fall time	—	15	—		
C_{iss}	Input capacitance	—	4300	—	pF	$V_{GS} = 0V$ $V_{DS} = -10V$ $f = 1MHz$
C_{oss}	Output capacitance	—	500	—		
C_{rss}	Reverse transfer capacitance	—	320	—		

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-50	A	MOSFET symb showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	-200	A	
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$I_S = -1A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	—	55	—	ns	$T_J = 25^{\circ}C, I_F = -20A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	365	—	nC	

Test circuits and Waveforms
EAS test circuits:

Gate charge test circuit:

Switch Time Test Circuit:

Switch Waveforms:

Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical electrical and thermal characteristics

Figure 1. Typical Output Characteristics

Figure 2. On-resistance Vs. G-S Voltage

Figure 3. Source Drain Forward Characteristics

Figure 4. Gate-Charge Characteristics

Figure 5. Normalized $V_{GS(th)}$ Vs T_J

Figure 6. Normalized $R_{DS(on)}$ Vs T_J

Typical electrical and thermal characteristics

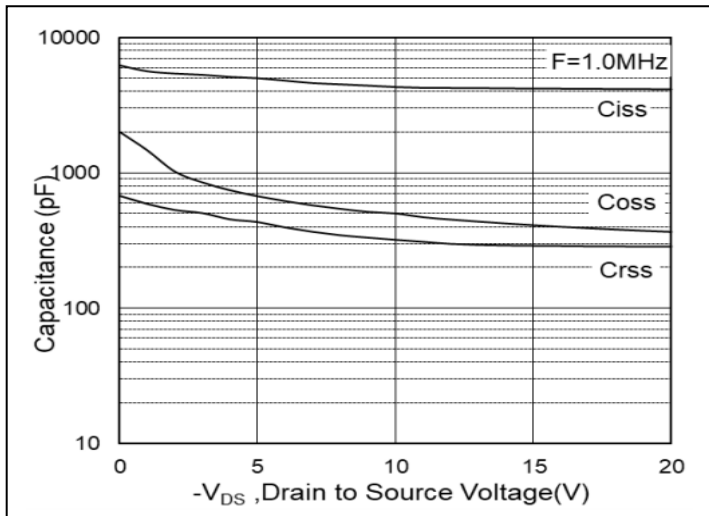


Figure 7. Capacitance

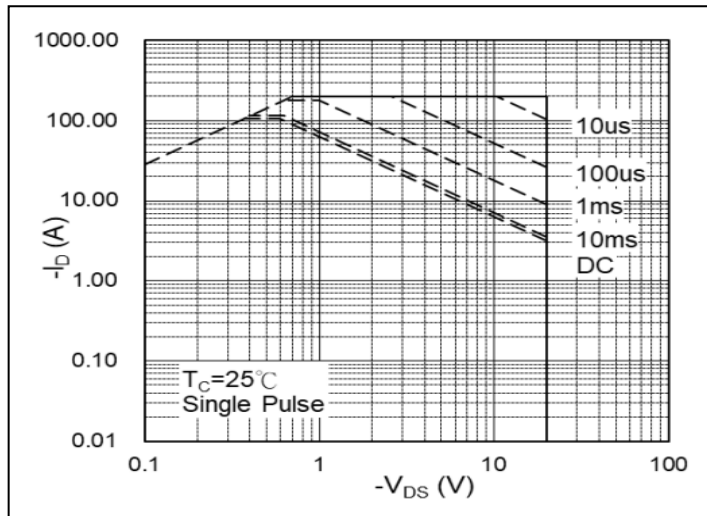


Figure 8. Safe Operating Area

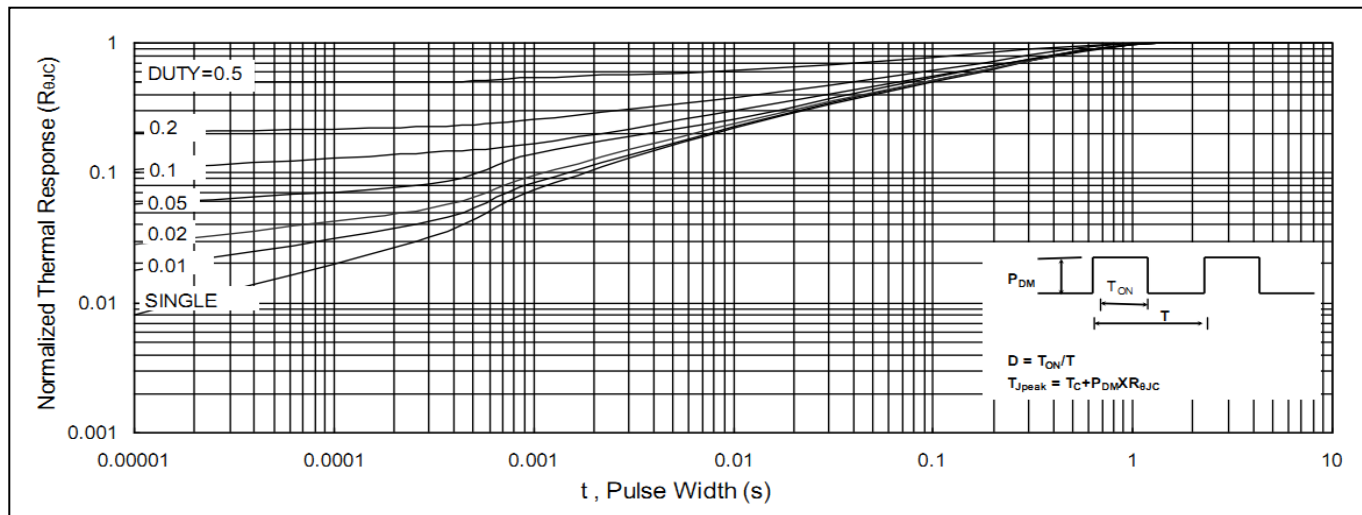
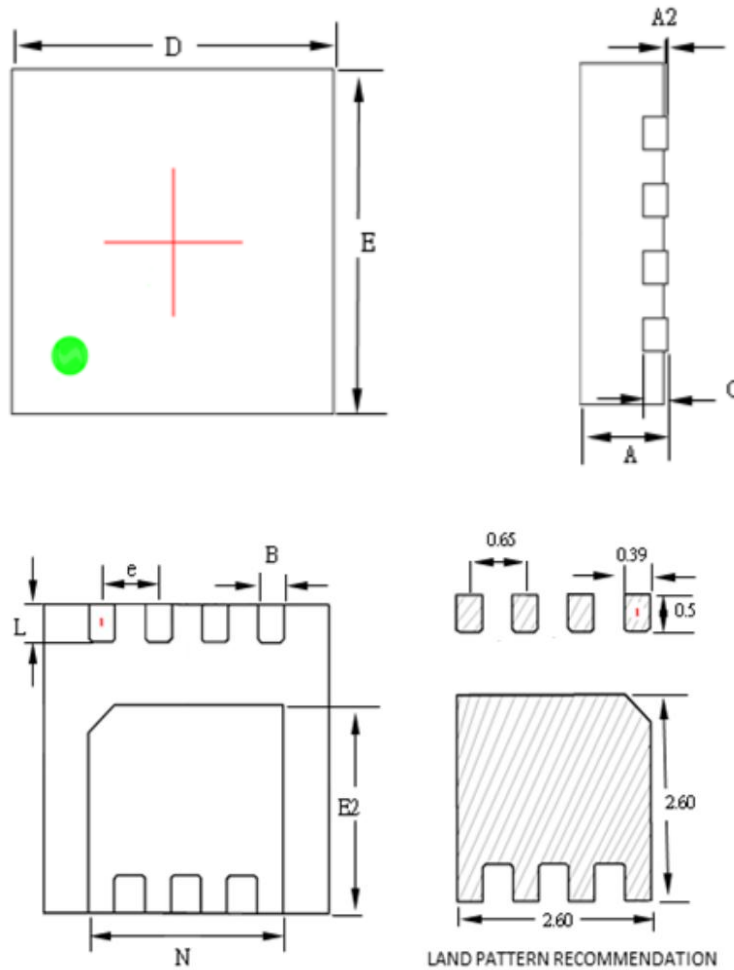


Figure 9. Normalized Maximum Transient Thermal Impedance

Mechanical Data:


SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A2	0.00	--	0.05	0.000	--	0.002
B	0.24	0.30	0.35	0.009	0.012	0.014
C	0.10	0.15	0.25	0.004	0.006	0.010
D	3.15	3.30	3.40	0.124	0.130	0.134
E	3.15	3.30	3.40	0.124	0.130	0.134
E2	2.15	2.25	2.35	0.085	0.089	0.093
L	0.35	0.40	0.45	0.014	0.016	0.018
N	2.10	2.25	2.35	0.083	0.089	0.093
e	--	0.65	--	--	0.026	--

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