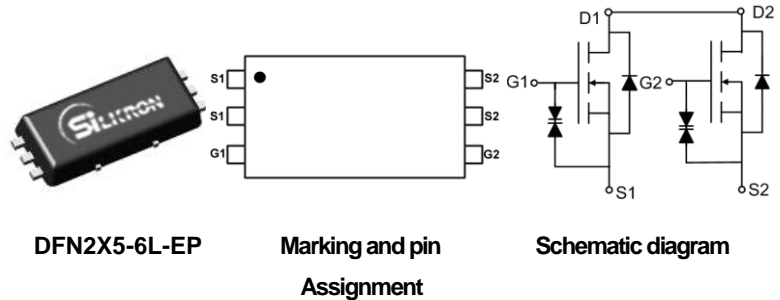


**Main Product Characteristics:**

$V_{DSS}$	20V
$R_{DS(on)}$	14.5mohm (typ.)
$I_D$	8.5A


**Features and Benefits:**

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


**Description:**

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

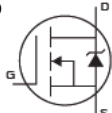
**Absolute max Rating:**

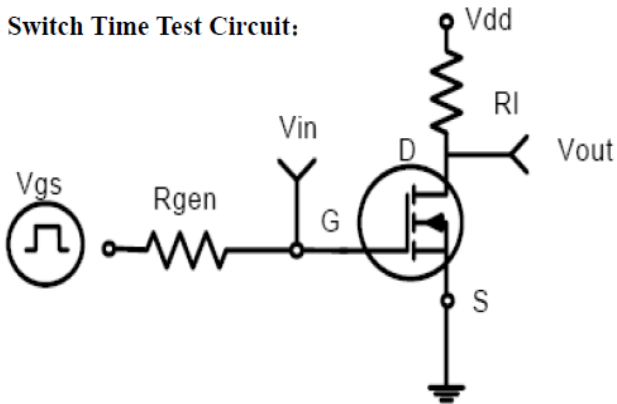
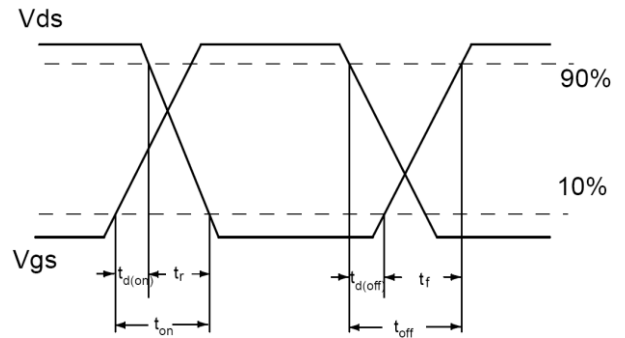
Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	8.5 ①	A
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	75 ①	
$I_{DM}$	Pulsed Drain Current ②	34	
$V_{GS}$	Gate to source voltage	$\pm 10$	V
$P_D @ TC = 25^\circ C$	Power Dissipation ③	1.3	W
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	$^\circ C$

**Electrical Characterizes @ $T_A=25^{\circ}\text{C}$  unless otherwise specified**

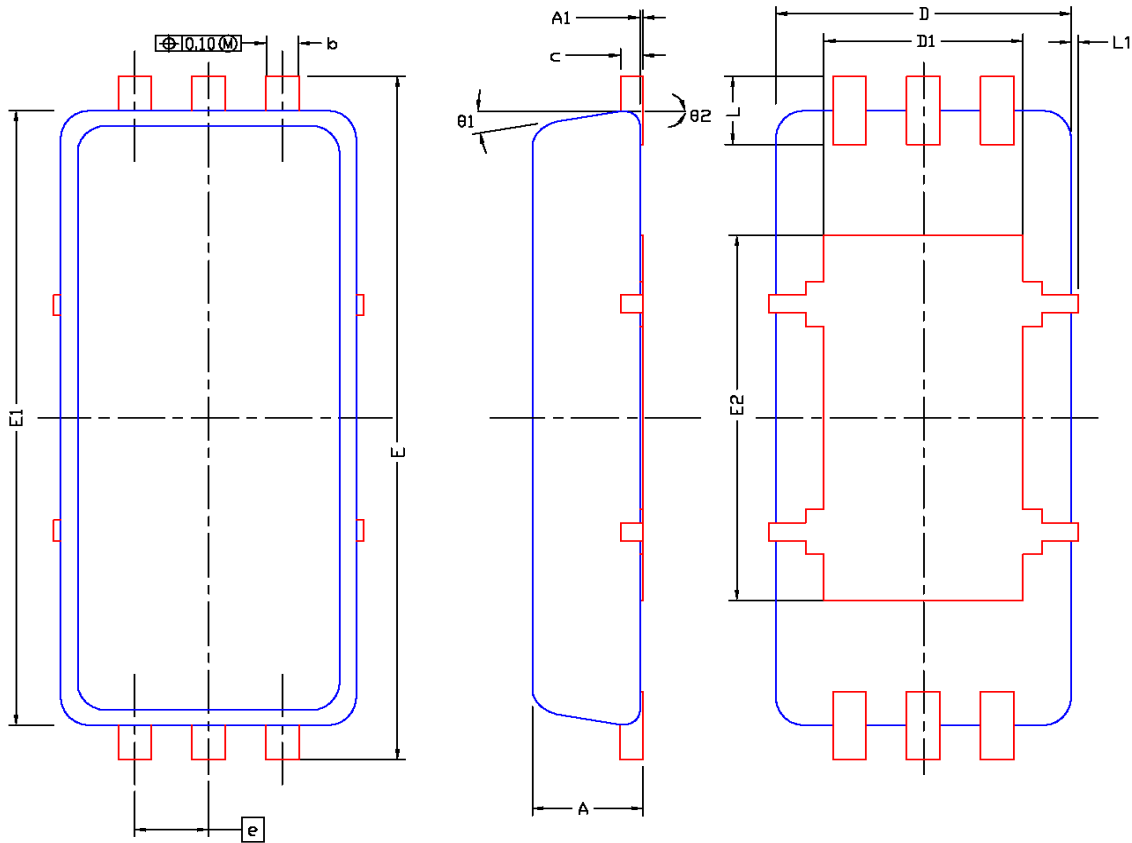
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	14.5	17.5	m $\Omega$	$V_{GS} = 4.5V, I_D = 4A$
		—	15.2	18.5		$V_{GS} = 4V, I_D = 4A$
		—	17.3	20		$V_{GS} = 3.1V, I_D = 4A$
		—	20.3	27.5		$V_{GS} = 2.5V, I_D = 4A$
$V_{GS(th)}$	Gate threshold voltage	0.5	—	1.45	V	$V_{DS} = V_{GS}, I_D = 1mA$
$I_{DSS}$	Drain-to-Source leakage current	—	—	1	$\mu A$	$V_{DS} = 20V, V_{GS} = 0V$
$I_{GSS}$	Gate-to-Source forward leakage	—	—	10	$\mu A$	$V_{GS} = 10V$
		—	—	-10		$V_{GS} = -10V$
$Q_g$	Total gate charge	—	8	—	nC	$I_D = 6A,$ $V_{DS} = 10V,$ $V_{GS} = 4.5V$
$Q_{gs}$	Gate-to-Source charge	—	1.5	—		
$Q_{gd}$	Gate-to-Drain("Miller") charge	—	2	—		
$t_{d(on)}$	Turn-on delay time	—	20	—	nS	$V_{DD} = 10V,$ $I_D = 1A,$ $R_G = 10\Omega,$ $V_{GS} = 4.5V$
$t_r$	Rise time	—	50	—		
$t_{d(off)}$	Turn-Off delay time	—	64	—		
$t_f$	Fall time	—	40	—		
$C_{iss}$	Input capacitance	—	650	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output capacitance	—	170	—		$V_{DS} = 10V$
$C_{riss}$	Reverse transfer capacitance	—	150	—		$f = 1MHz$

**Source-Drain Ratings and Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_s$	Continuous Source Current	—	—	8.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current	—	—	34	A	
$V_{SD}$	Diode Forward Voltage	—	0.7	1.3	V	$I_s = 1.5A, V_{GS} = 0V$

**Test circuits and Waveforms**
**Switch Time Test Circuit:**

**Switching time waveform:**

**Notes:**

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

**Mechanical Data:**
**DFN2X5-6L-EP PACKAGE OUTLINE DIMENSION :**


Dim.	Millimeters			Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.0315
A1	0.00	---	0.05	0.000	---	0.002
b	0.20	0.225	0.30	0.008	0.009	0.012
c	0.10	0.152	0.20	0.004	0.006	0.008
D	2.00 BSC			0.079 BSC		
D1	1.30	1.35	1.55	0.051	0.053	0.061
E	5.00 BSC			0.197 BSC		
E1	4.50 BSC			0.177 BSC		
E2	2.60	2.67	2.95	0.102	0.105	0.116
e	0.50 BSC			0.020 BSC		
L	0.40	0.50	0.60	0.016	0.0197	0.0236
L1	0	---	0.100	0	---	0.004
$\theta 1$	0°	10°	12°	0°	10°	12°
$\theta 2$	3° BSC			3° BSC		

**Ordering and Marking Information**
**Device Marking: 2116EJ3**

**Package (Available)**  
**DFN2X5-6L-EP**  
**Operating Temperature Range**  
**C : -55 to 150 °C**

**Devices per Unit**

Package Type	Units/ Tape	Tapes/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
DFN2X5-6L-EP	3000pcs	4pcs	12000pcs	4pcs	48000pcs

**Reliability Test Program**

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to $150^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices

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