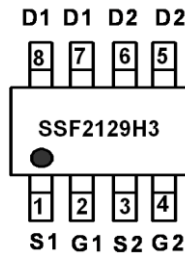
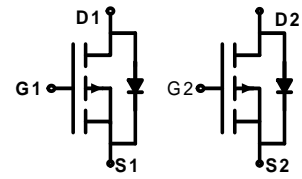


Main Product Characteristics:

V_{DSS}	-20V
$R_{DS(on)}$	21m Ω (typ.)
I_D	-6.0A


SOP-8

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V ^①	-6	A
I_{DM}	Pulsed Drain Current ^②	-24	
P_D @TC = 25°C	Power Dissipation ^③	2.0	W
	Linear Derating Factor	0.016	W/°C
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	±8	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

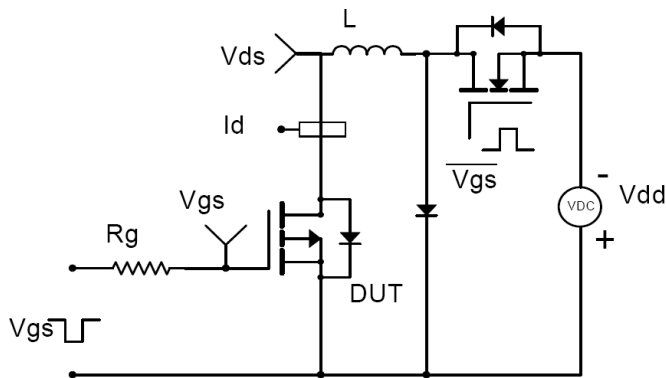
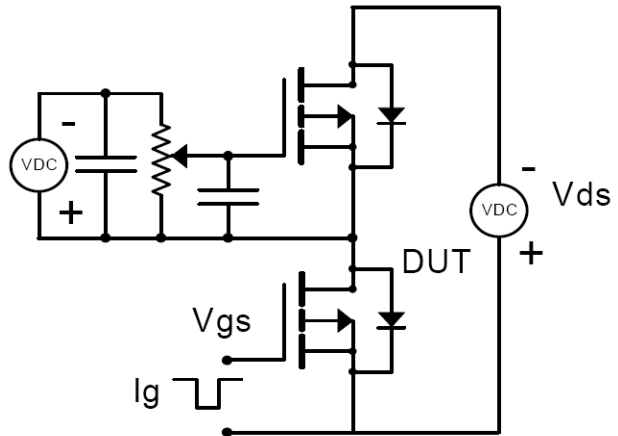
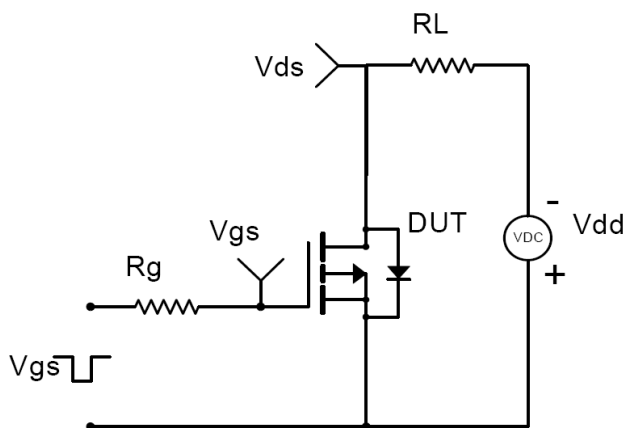
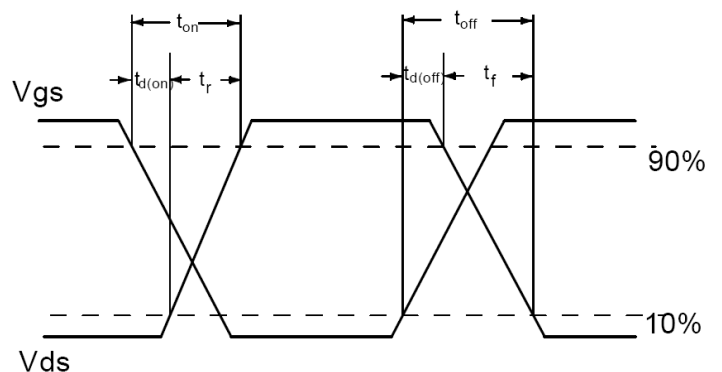
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^③	—	40	°C/W
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ^④	—	78	°C/W

Electrical Characterizes @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	21	30	m Ω	$V_{GS}=-4.5V, I_D = -6A$
		—	33	40	m Ω	$V_{GS}=-2.5V, I_D = -5.3A$
$V_{GS(th)}$	Gate threshold voltage	-0.4	—	-1.5	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = -20V, V_{GS} = 0V$ $T_J = 125^{\circ}\text{C}$
		—	—	50		
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 8V$
		—	—	-100		$V_{GS} = -8V$
Q_g	Total gate charge	—	24	—	nC	$I_D = -6A,$ $V_{DS}=-10V,$ $V_{GS} = -5V$
Q_{gs}	Gate-to-Source charge	—	4.2	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	5.6	—		
$t_{d(on)}$	Turn-on delay time	—	8.1	—	ns	$V_{GS}=-4.5V, V_{DS}=-10V,$ $I_D = -1A,$ $R_{GEN}=6\Omega$
t_r	Rise time	—	15.2	—		
$t_{d(off)}$	Turn-Off delay time	—	98	—		
t_f	Fall time	—	35	—		
C_{iss}	Input capacitance	—	2819	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	262	—		$V_{DS} = -10V$
C_{riss}	Reverse transfer capacitance	—	196	—		$f = 1\text{MHz}$

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	-24	A	
V_{SD}	Diode Forward Voltage	—	—	-1.0	V	$I_S=-2.9A, V_{GS}=0V$

Test circuits and Waveforms
EAS test circuit:

Gate charge test circuit:

Switching time test circuit:

Switch Waveforms:

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max junction temperature.
- ③ The value of R_{θJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C
- ④ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)} = 150°C.

Typical electrical and thermal characteristics

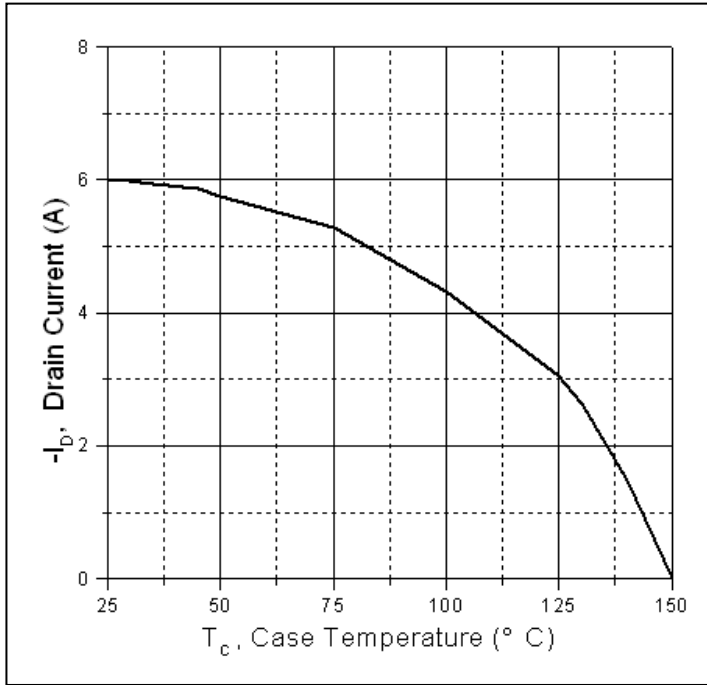


Figure 1. Maximum Drain Current Vs. Case Temperature

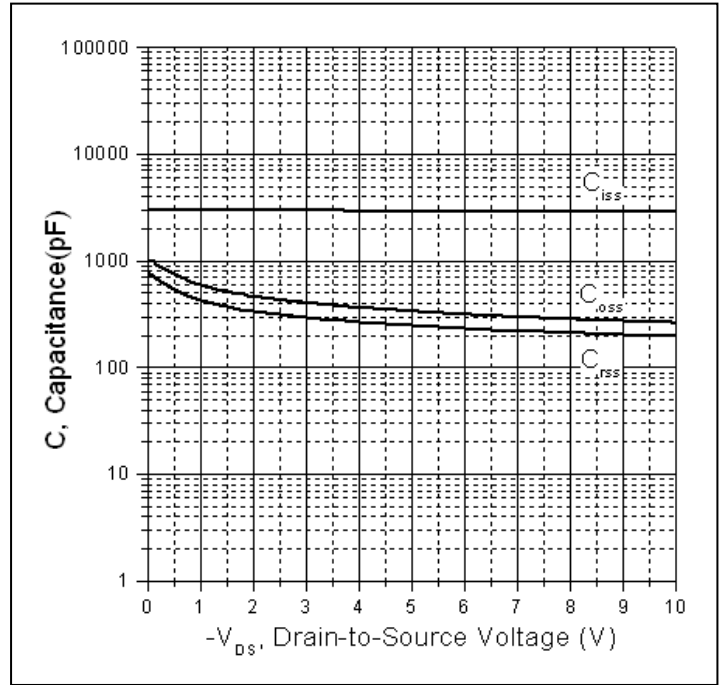


Figure 2. Typical Capacitance Vs. Drain-to-Source Voltage

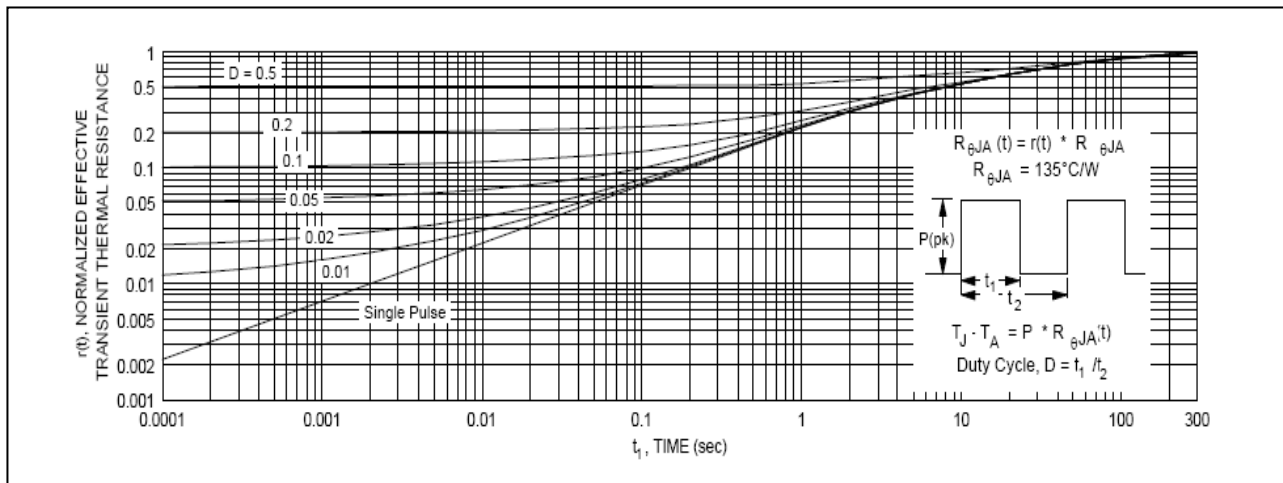
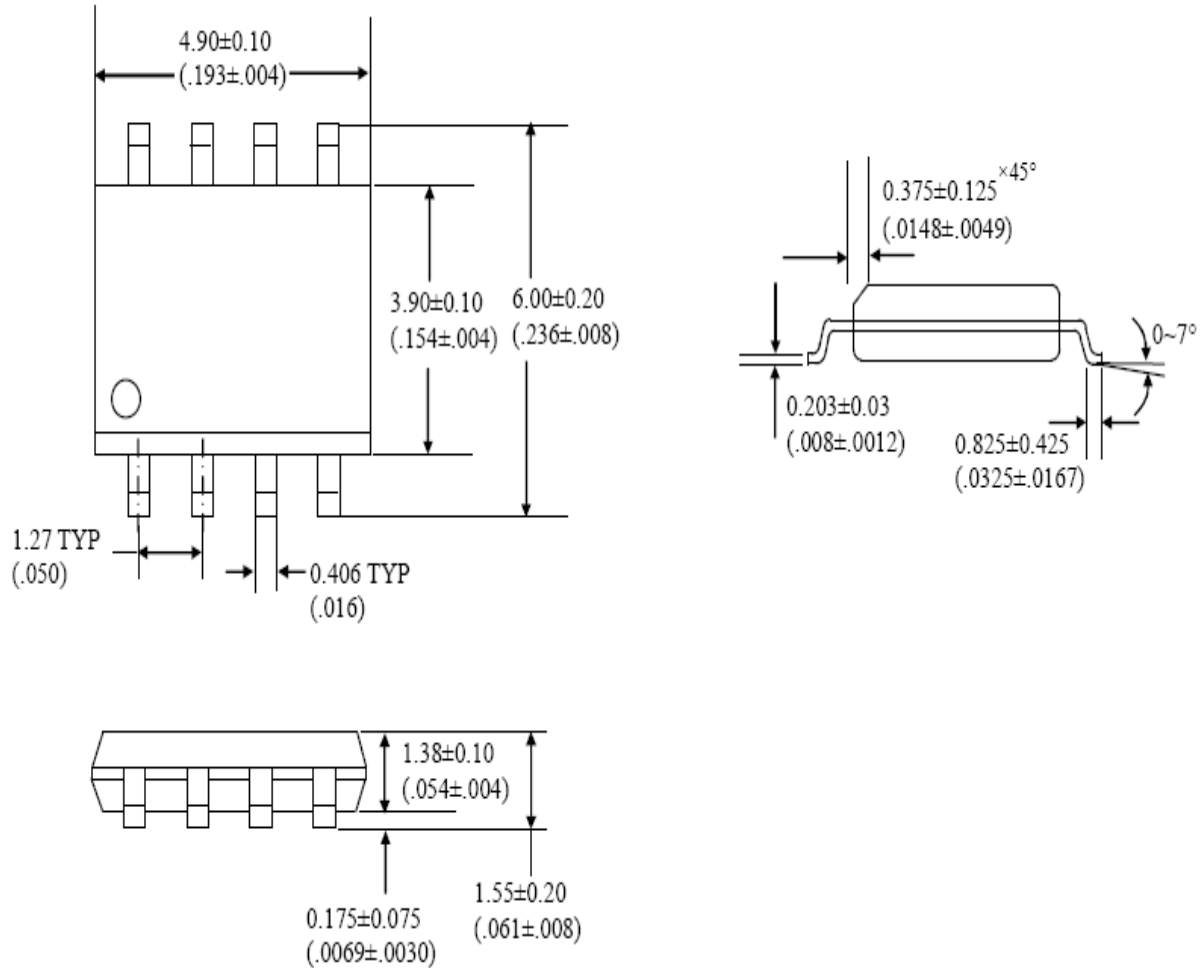


Figure3. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:
SOP8 PACKAGE OUTLINE DIMENSION


Ordering and Marking Information
Device Marking: SSF2129H3

Package (Available)
SOP-8
Operating Temperature Range
C : -55 to 150 °C

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
SOP-8	2500	2	5000	8	40000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ or 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=125^{\circ}\text{C}$ or 150°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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