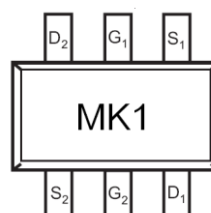
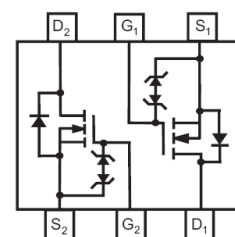


**Main Product Characteristics:**

$V_{DSS}$	20V
$R_{DS(on)}$	0.4Ω (typ.)
$I_D$	0.54A


**SOT-363**

**Marking and Pin Assignment**

**Schematic Diagram**
**Features and Benefits:**

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


**Description:**

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

**Absolute max Rating:**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±8	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	I <sub>D</sub>	0.54	A
	I <sub>DM</sub>	1.5	A
Maximum Power Dissipation	P <sub>D</sub>	0.2	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 To 150	°C

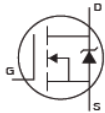
**Thermal Resistance**

Thermal Resistance, Junction-to-Ambient (Note 2)	R <sub>θJA</sub>	625	°C/W
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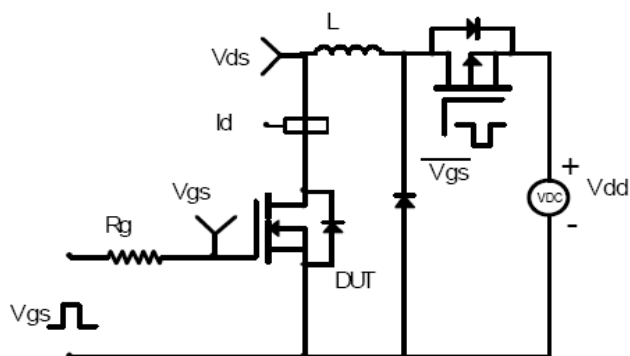
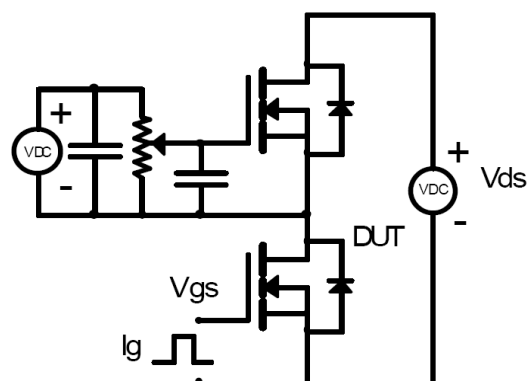
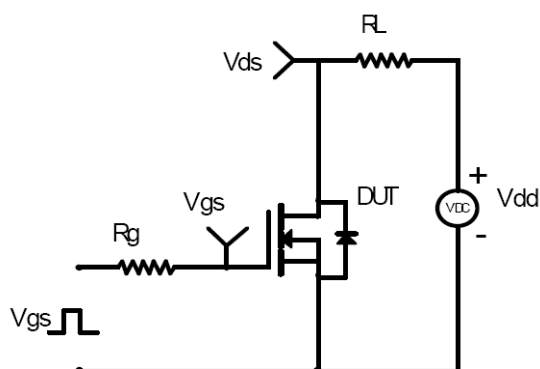
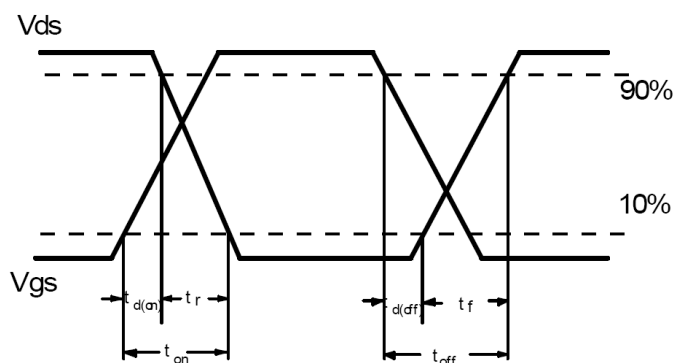
**Electrical Characteristics** @ $T_A=25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.4	0.55	$\Omega$	$V_{GS}=4.5V, I_D = 0.54A$
		—	0.5	0.7	$\Omega$	$V_{GS}=2.5V, I_D = 0.5A$
		—	0.7	0.9	$\Omega$	$V_{GS}=1.8V, I_D = 0.35A$
$V_{GS(th)}$	Gate threshold voltage	0.5	—	1.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source leakage current	—	—	1	$\mu A$	$V_{DS} = 20V, V_{GS} = 0V$
$I_{GSS}$	Gate-to-Source forward leakage	—	—	$\pm 1$	$\mu A$	$V_{GS} = \pm 4.5V$
		—	—	$\pm 10$		$V_{GS} = \pm 8V$
$C_{iss}$	Input capacitance	—	87	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output capacitance	—	17	—		$V_{DS} = 16V$
$C_{rss}$	Reverse transfer capacitance	—	10	—		$f = 1MHz$

**Source-Drain Ratings and Characteristics**

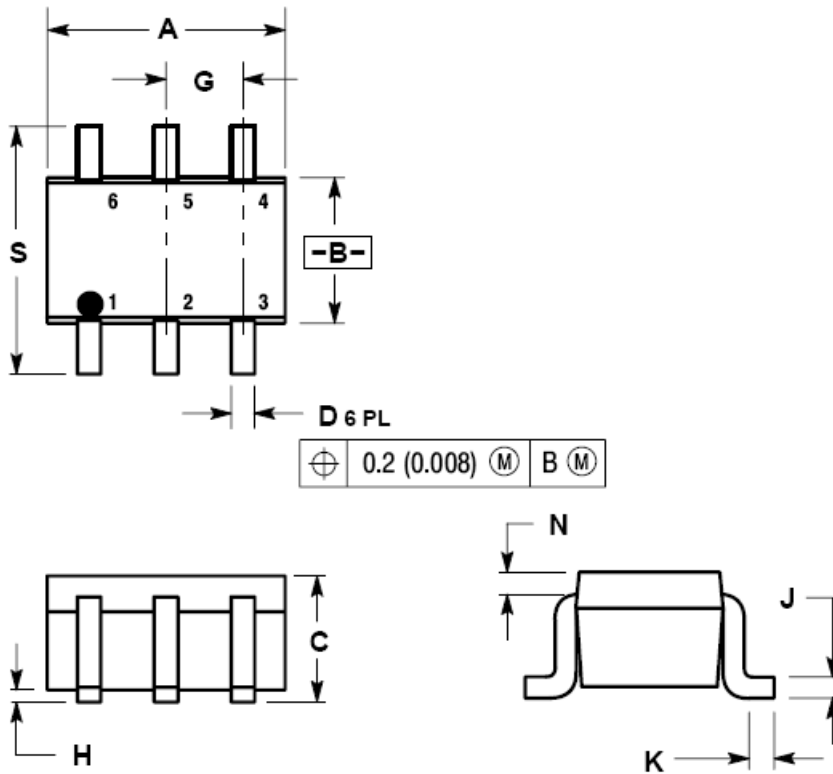
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	0.54	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)	—	—	1.5	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	

## Test circuits and Waveforms

**EAS Test Circuit**

**Gate charge test circuit**

**Switching Time Test Circuit**

**Switching Waveforms**


### Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$

**Mechanical Data:**
**SOT-363(SC-88) PACKAGE OUTLINE DIMENSION**

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

**Ordering and Marking Information**

<b>Device Marking: MK1</b>  <div style="text-align: center;"> <b>Package (Available)</b>  <b>SOT-363(SC-88)</b>  <b>Operating Temperature Range</b>  <b>C : -55 to 150 °C</b> </div>
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**Devices per Unit**

Package Type	Units/Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/ Carton Box
SOT-363	3000	10	30000	12	360000

**Reliability Test Program**

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to $150^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices

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