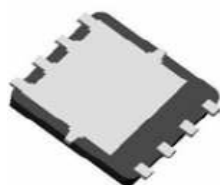
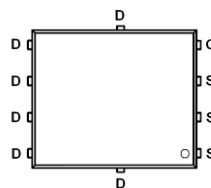
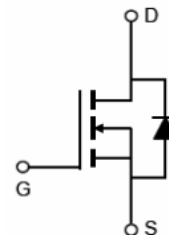


Main Product Characteristics:

| | |
|--------------|----------------------|
| V_{DSS} | 60V |
| $R_{DS(on)}$ | 4.3m Ω (typ.) |
| I_D | 116A |


PQFN 5x6

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating:

| Symbol | Parameter | Max. | Units |
|-------------------|--|-------------|-------|
| I_D @ TC = 25°C | Continuous Drain Current, V_{GS} @ 10V ① | 116 | A |
| I_{DM} | Pulsed Drain Current ② | 250 | |
| P_D @TC = 25°C | Power Dissipation ③ | 113 | W |
| V_{DS} | Drain-Source Voltage | 60 | V |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy @ L=0.1mH | 125 | mJ |
| T_J T_{STG} | Operating Junction and Storage Temperature Range | -55 to +150 | °C |

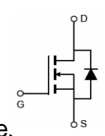
Thermal Resistance

| Symbol | Characterizes | Typ. | Max. | Units |
|-----------------|--|------|------|---------------|
| $R_{\theta JC}$ | Junction-to-case ③ | — | 1.1 | $^{\circ}C/W$ |
| $R_{\theta JA}$ | Junction-to-ambient ($t \leq 10s$) ④ | — | 62 | $^{\circ}C/W$ |

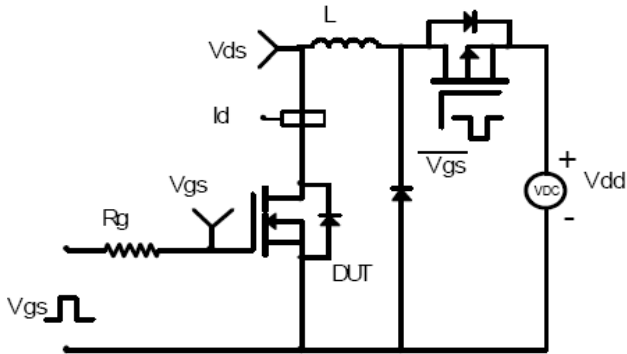
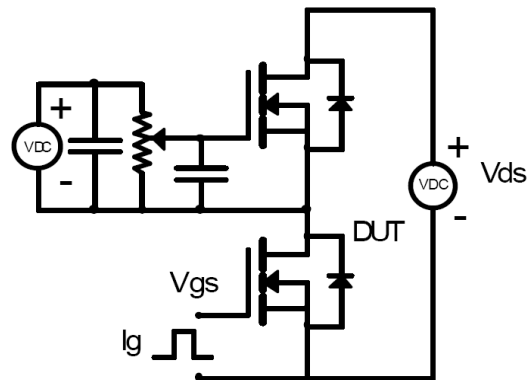
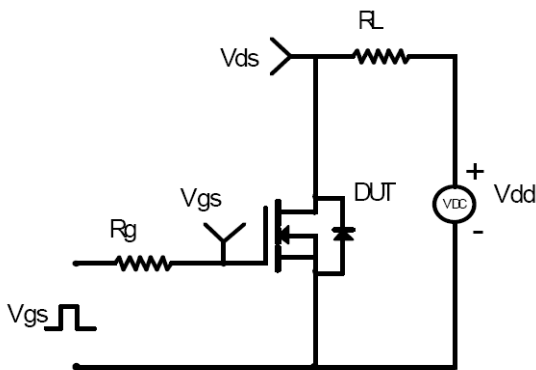
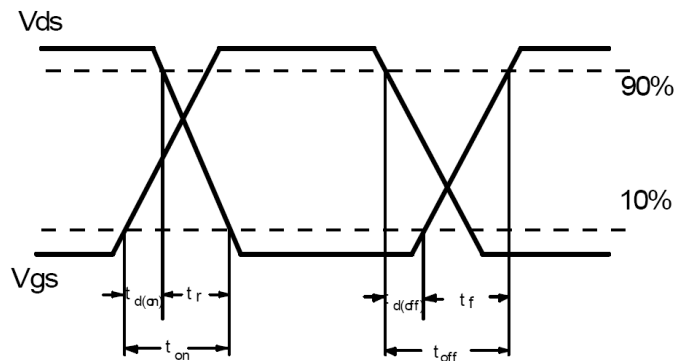
Electrical Characterizes @ $T_A=25^{\circ}C$ unless otherwise specified

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------|--------------------------------------|------|------|------|------------|---|
| $V_{(BR)DSS}$ | Drain-to-Source breakdown voltage | 60 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $R_{DS(on)}$ | Static Drain-to-Source on-resistance | — | 4.3 | 6 | m Ω | $V_{GS}=10V, I_D=15A$ |
| | | — | 6 | 7 | | $V_{GS}=4.5V, I_D=10A$ |
| $V_{GS(th)}$ | Gate threshold voltage | 1.2 | — | 2.5 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| I_{DSS} | Drain-to-Source leakage current | — | — | 1 | μA | $V_{DS} = 48V, V_{GS} = 0V$ |
| I_{GSS} | Gate-to-Source forward leakage | — | — | 100 | nA | $V_{GS} = 20V$ |
| | | — | — | -100 | | $V_{GS} = -20V$ |
| Q_g | Total gate charge | — | 72 | — | nC | $I_D = 25A,$ $V_{DS}=48V,$ $V_{GS} = 10V$ |
| Q_{GS} | Gate-to-Source charge | — | 13 | — | | |
| Q_{gd} | Gate-to-Drain("Miller") charge | — | 18 | — | | |
| $t_{d(on)}$ | Turn-on delay time | — | 19 | — | ns | $V_{GS}=10V, V_{DS}=30V,$ $R_{GEN}=3.3\Omega$ $I_D = 30A$ |
| t_r | Rise time | — | 9 | — | | |
| $t_{d(off)}$ | Turn-Off delay time | — | 59 | — | | |
| t_f | Fall time | — | 16 | — | | |
| C_{iss} | Input capacitance | — | 4700 | — | pF | $V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1MHz$ |
| C_{oss} | Output capacitance | — | 320 | — | | |
| C_{riss} | Reverse transfer capacitance | — | 240 | — | | |

Source-Drain Ratings and Characteristics

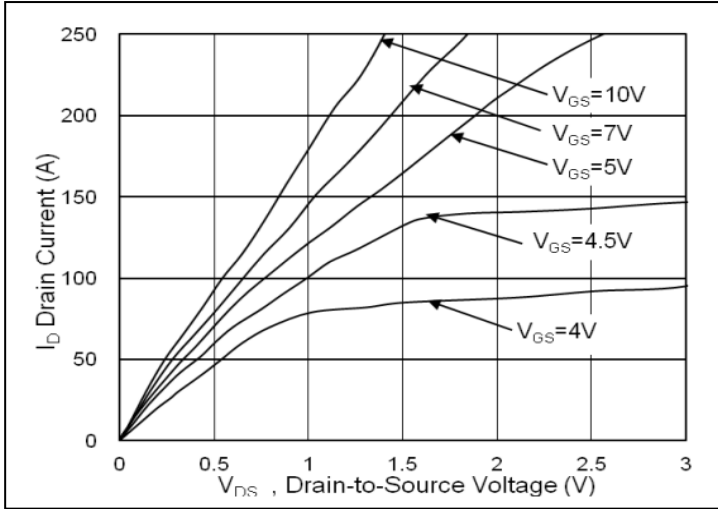
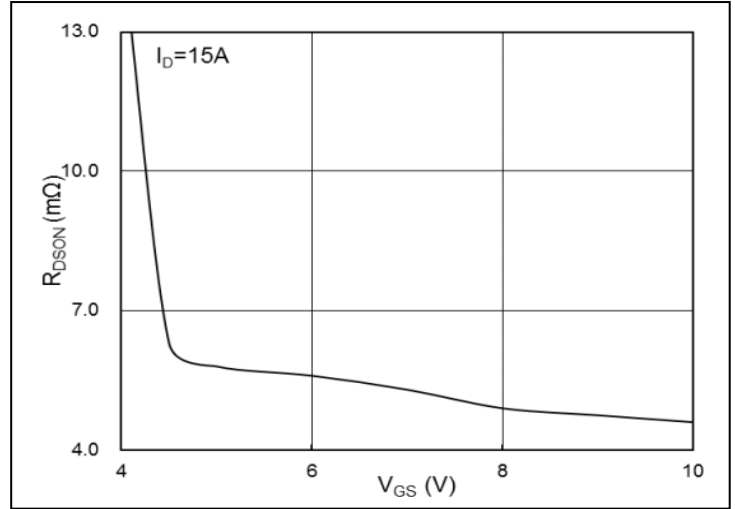
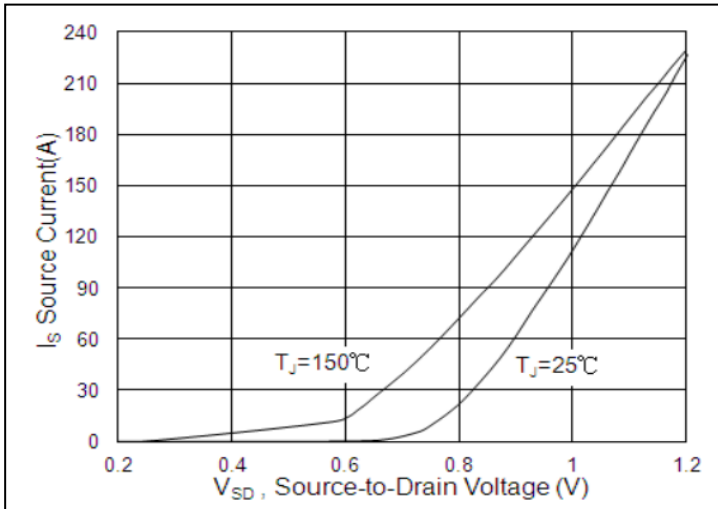
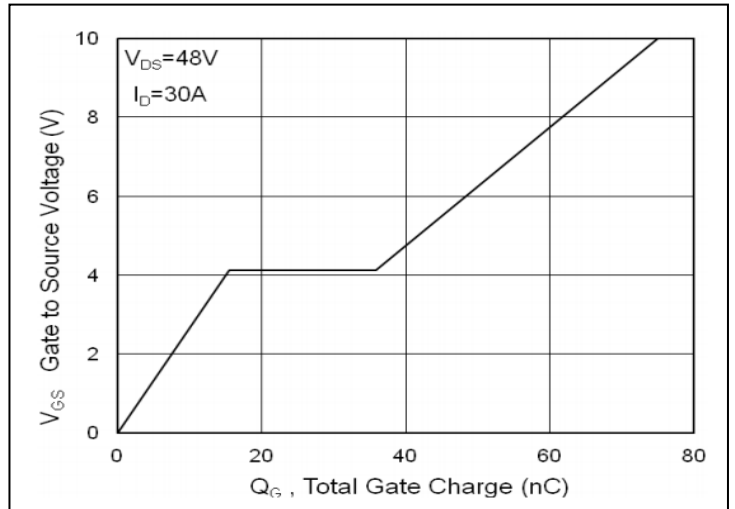
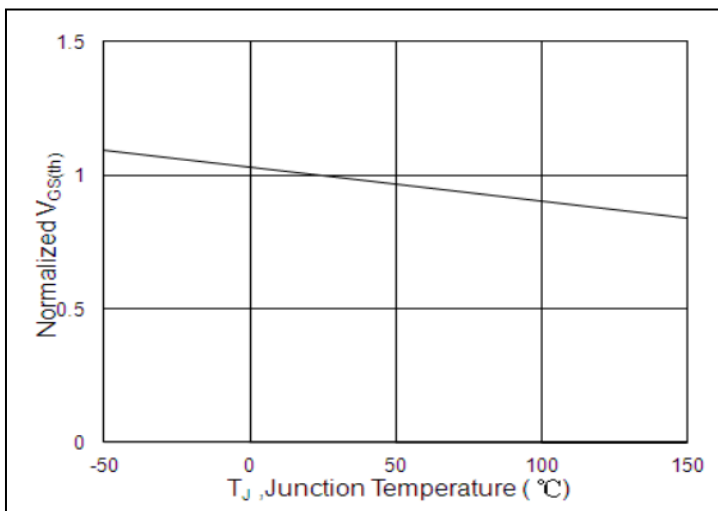
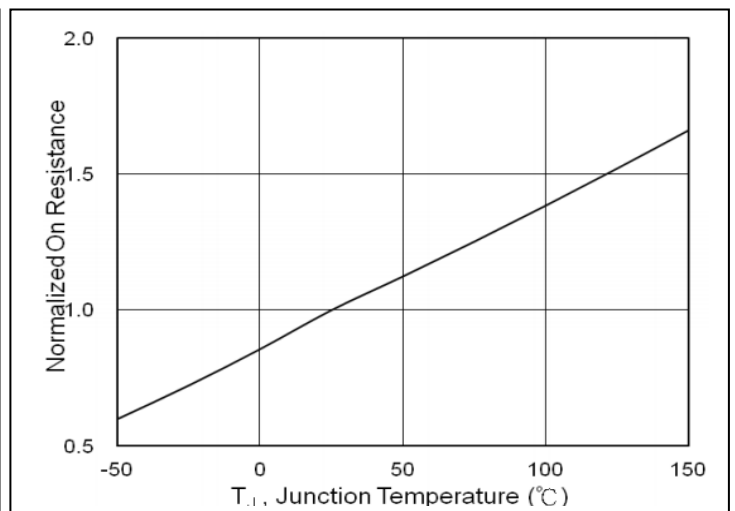
| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|------|------|------|-------|--|
| I_S | Continuous Source Current (Body Diode) | — | — | 116 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I_{SM} | Pulsed Source Current (Body Diode) | — | — | 250 | A | |
| V_{SD} | Diode Forward Voltage | — | — | 1.2 | V | $I_S=1A, V_{GS}=0V$ |
| t_{rr} | Reverse Recovery Time | — | 23 | — | ns | $I_S=30A, di/dt=100A/us$ |
| Q_{rr} | Reverse Recovery Charge | — | 12 | — | nC | |

Test circuits and Waveforms

EAS Test Circuit:

Gate charge test circuit:

Switching Time Test Circuit:

Switching Waveforms:


Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical electrical and thermal characteristics

Figure 1: Typical Output Characteristics

Figure 2: $R_{DS(on)}$ vs. V_{GS}

Figure 3: Diode Forward Voltage vs. Current

Figure 4: Gate-Charge Characteristics

Figure 5: $V_{GS(th)}$ vs. Junction Temperature

Figure 6: $R_{DS(on)}$ vs. Junction Temperature

Typical electrical and thermal characteristics

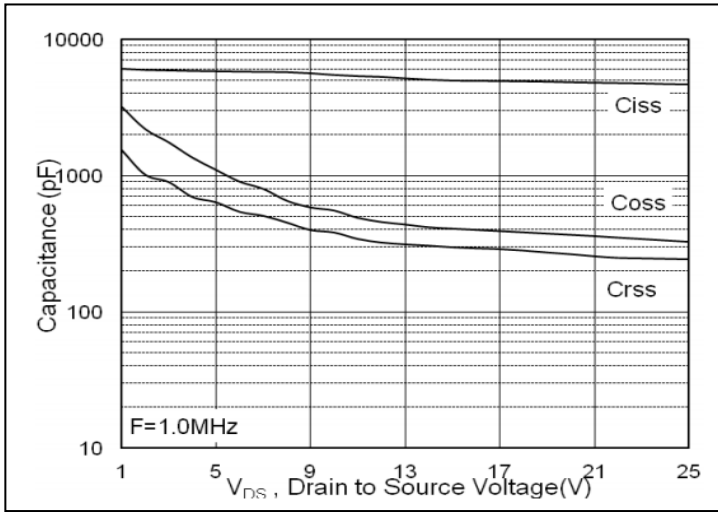


Figure 7: Capacitance

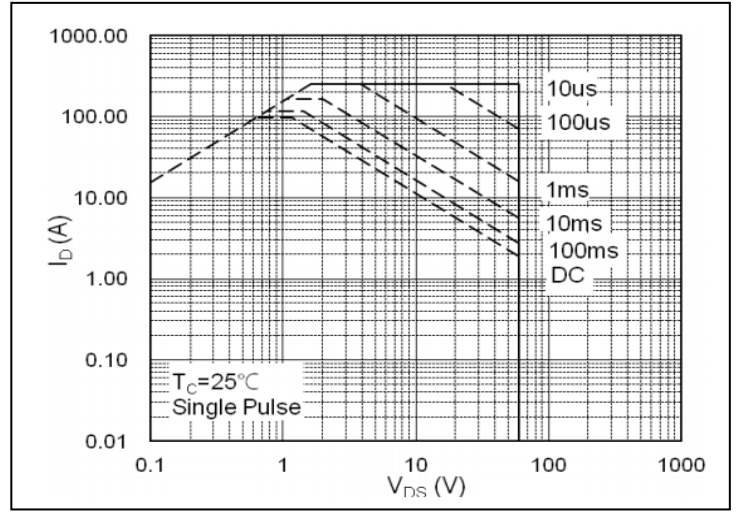


Figure 8: Safe Operation Area

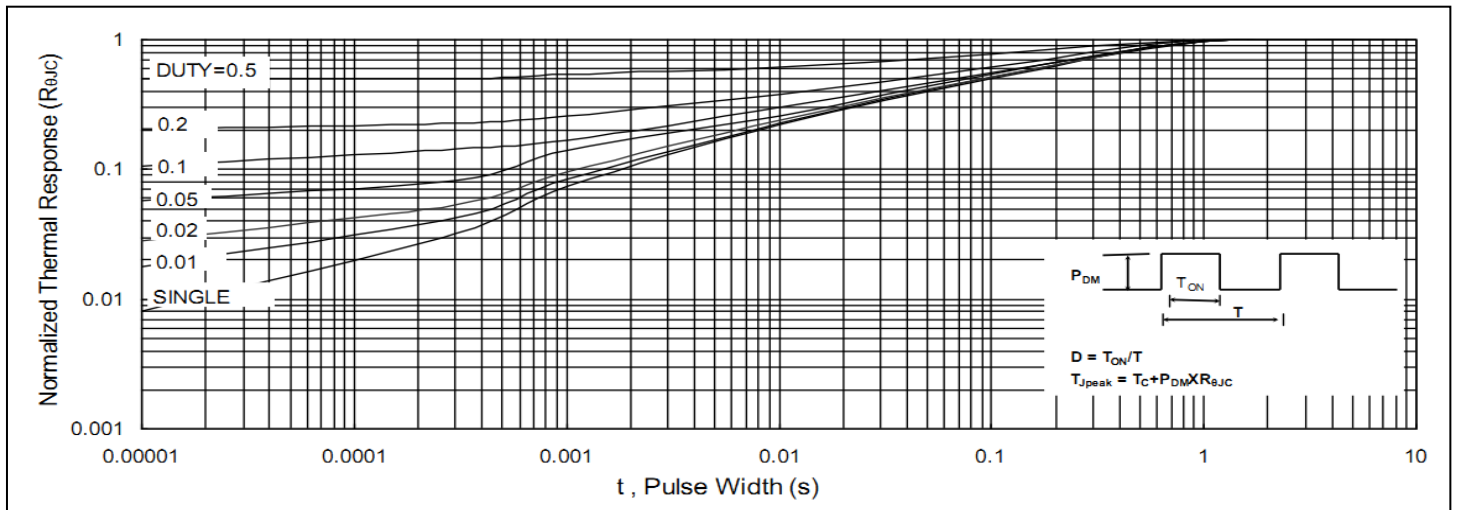
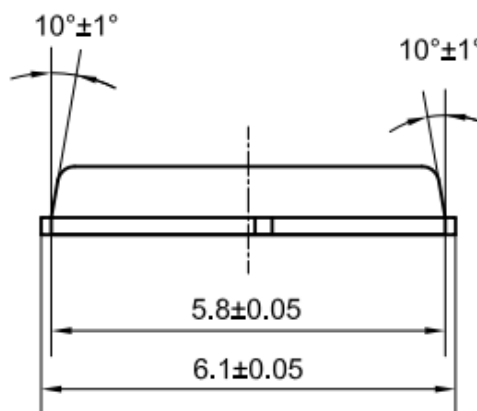
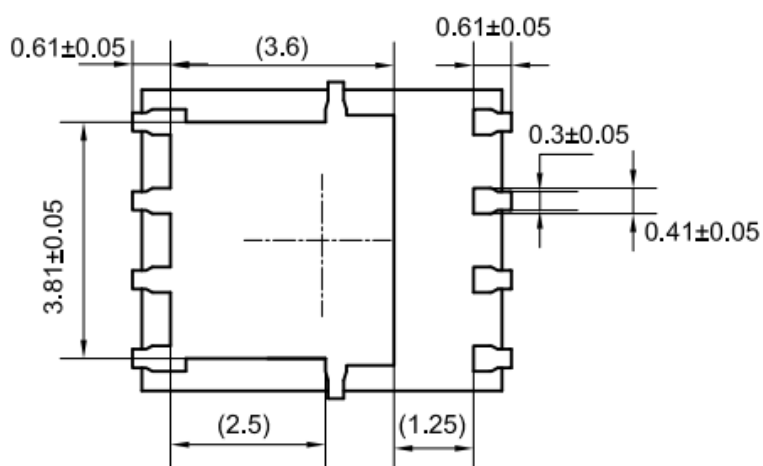
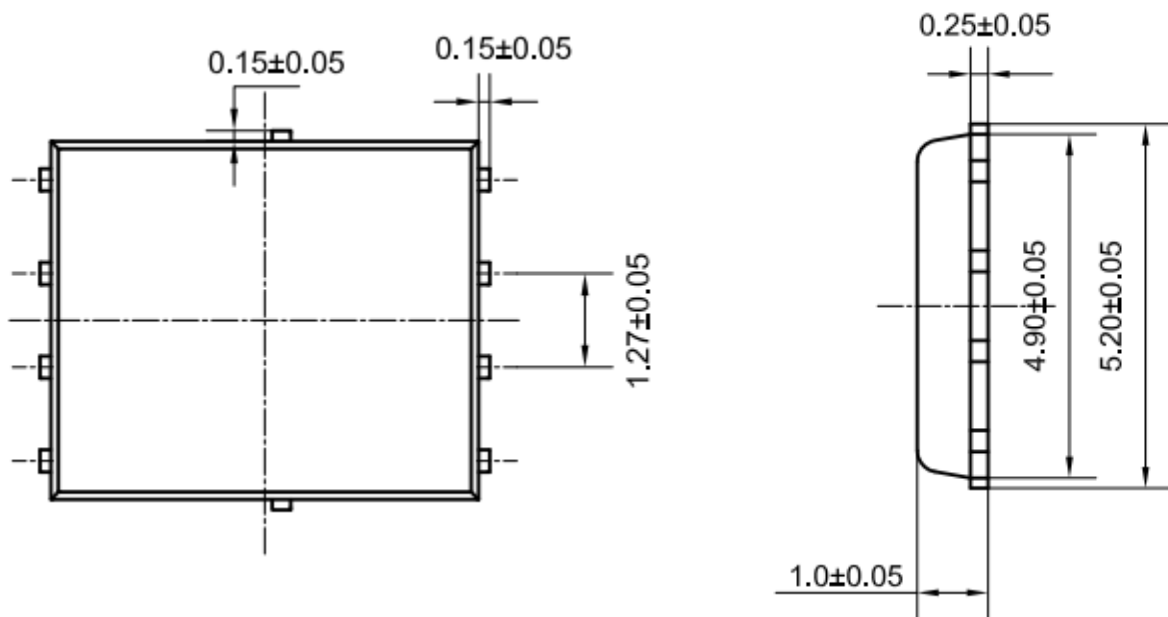


Figure 9: Normalized Maximum Transient Thermal Impedance

Mechanical Data:


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Suzhou Silikron Semiconductor Corp.

501 , NW-20,Nanopolis, 99th Jinjihu Avenue ,Industrial Park ,Suzhou ,P.R, CHINA

TEL: (86-512) 62560688

FAX: (86-512) 62560688-8092

E-mail: Sales@silikron.com