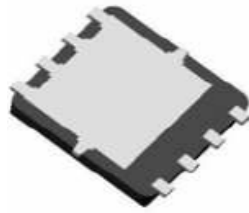
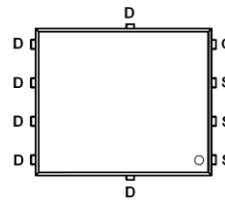
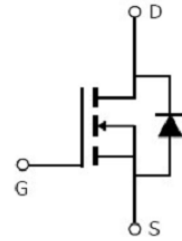


Main Product Characteristics:

V_{DSS}	60V
$R_{DS(on)}$	14m Ω (typ.)
I_D	60A


PQFN 5x6

Pin Assignment

Schematic Diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V ①	60	A
I_{DM}	Pulsed Drain Current ②	240	
P_D @TC = 25°C	Power Dissipation ③	115	W
	Linear Derating Factor	0.74	W/°C
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.3mH	235	mJ
I_{AS}	Avalanche Current @ L=0.3mH	39	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

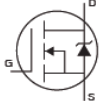
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^③	—	1.31	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-ambient ^④	—	62	$^{\circ}C/W$

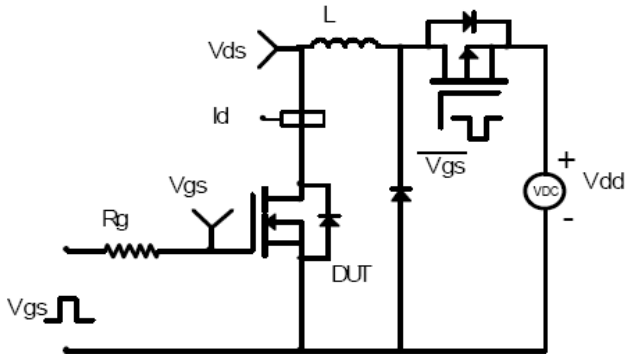
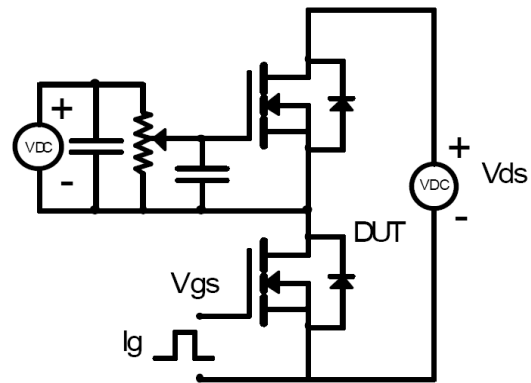
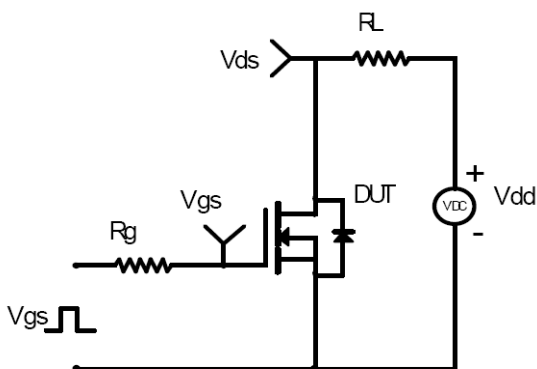
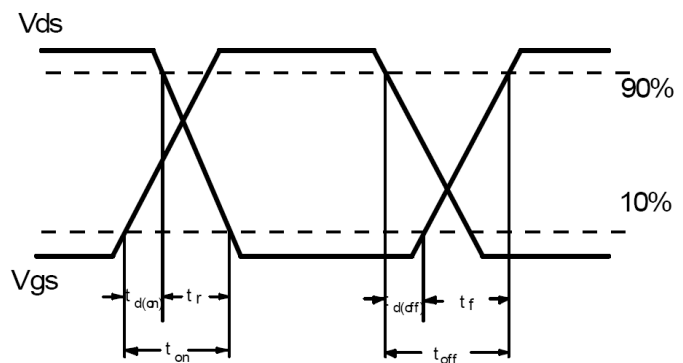
Electrical Characteristics @ $T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	14	16	m Ω	$V_{GS}=10V, I_D = 30A$
$V_{GS(th)}$	Gate threshold voltage	1	—	3	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 60V, V_{GS} = 0V$ $T_J = 150^{\circ}C$
		—	—	10		
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
Q_g	Total gate charge	—	45	—	nC	$I_D = 15A,$ $V_{DS}=30V,$ $V_{GS} = 10V$
Q_{GS}	Gate-to-Source charge	—	4	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	15	—		
$t_{d(on)}$	Turn-on delay time	—	15	—	ns	$V_{GS}=10V, V_{DS}=30V,$ $R_L=15\Omega,$ $R_{GEN}=2.5\Omega$
t_r	Rise time	—	14	—		
$t_{d(off)}$	Turn-Off delay time	—	40	—		
t_f	Fall time	—	7.3	—		
C_{iss}	Input capacitance	—	1480	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1MHz$
C_{oss}	Output capacitance	—	190	—		
C_{riss}	Reverse transfer capacitance	—	135	—		

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	40	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	80	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$I_S=30A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	33	—	ns	$T_J = 25^{\circ}C, I_F = 15A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	61	—	nC	

Test Circuits and Waveforms

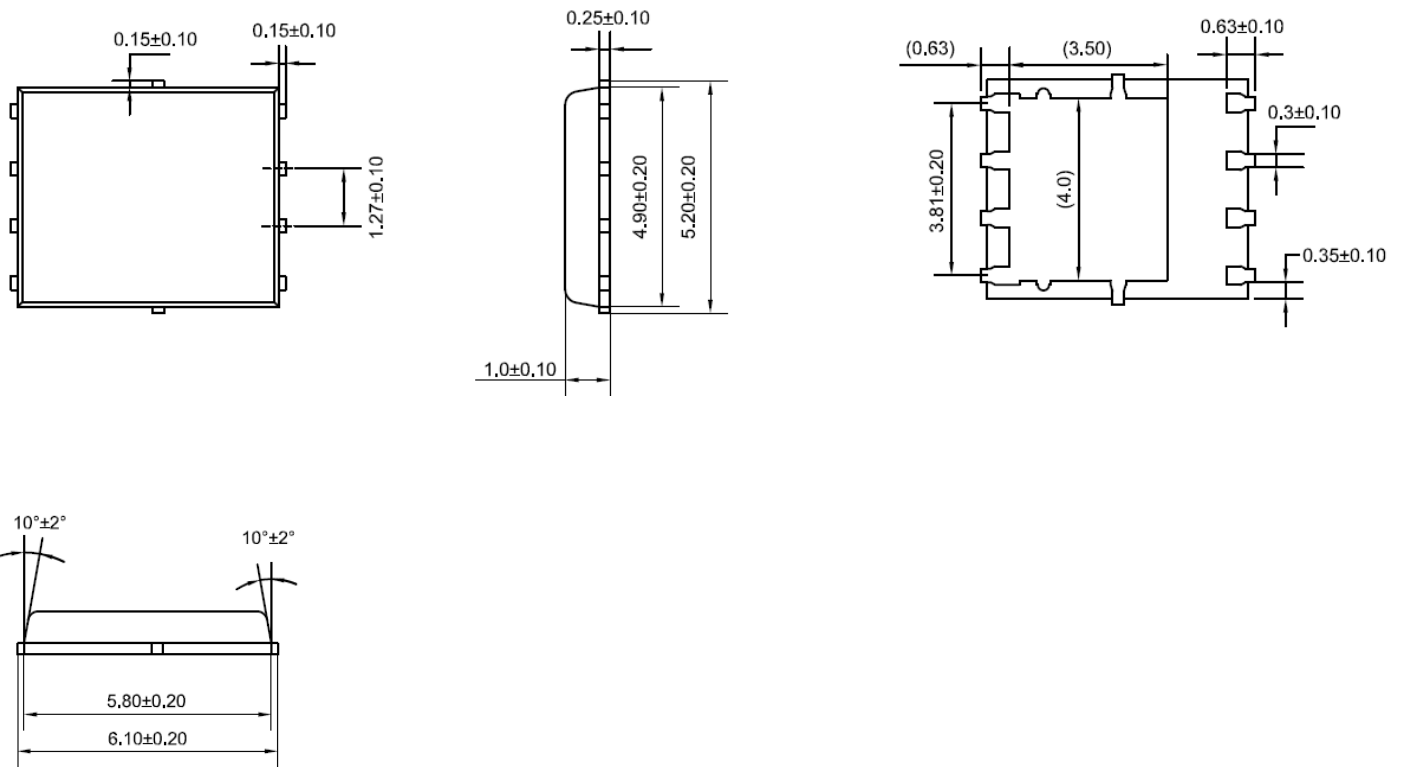
EAS Test Circuit

Gate charge test circuit

Switching Time Test Circuit

Switching Waveforms


Notes:

- ① Continuous current tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Mechanical Data

PQFN 5X6 Package Outline Dimension. (Unit: mm)



Ordering and Marking Information
Device Marking: SSF6014J7

Package (Available)
PQFN 5X6
Operating Temperature Range
C : -55 to 175 °C

Devices per Unit

Package Type	Units/Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
PQFN 5x6	3000	10	30000	4	120000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=150^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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Customer Service**Worldwide Sales and Service:**

Sales@silikron.com

Technical Support:

Technical@silikron.com

Suzhou Silikron Semiconductor Corp.

Building 11A Suchun Industrial Square, 428# Xinglong Street, Suzhou P.R. China

TEL: (86-512) 62560688

FAX: (86-512) 65160705

E-mail: Sales@silikron.com