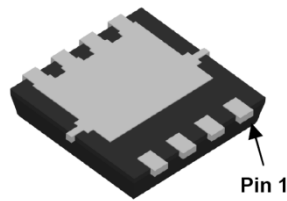
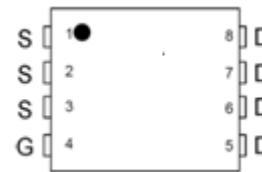
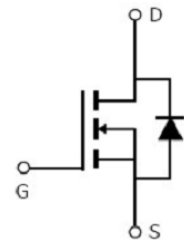


Main Product Characteristics:

V_{DS}	60V
$R_{DS(on)}$	12m Ω (typ.)
I_D	38A


DFN3.3x3.3
Bottom view

Pin Assignment

Schematic diagram
Features and Benefits:

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

Absolute max Rating:

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	38	A
I_{DM}	Pulsed Drain Current②	110	
$P_D @ TC = 25^\circ C$	Power Dissipation③	48	W
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ $L=0.3mH$ ②	60	mJ
I_{AR}	Avalanche Current @ $L=0.3mH$ ②	20	A
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ C$

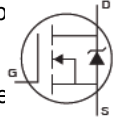
Thermal Resistance

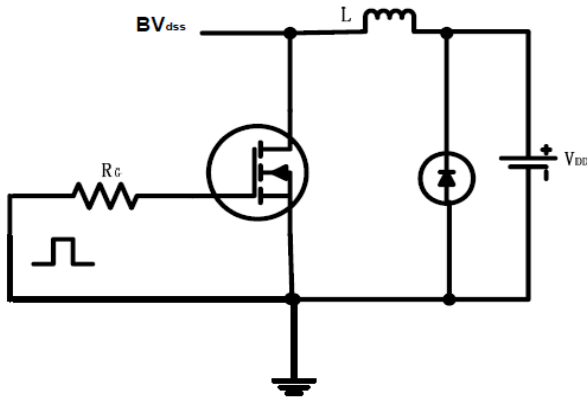
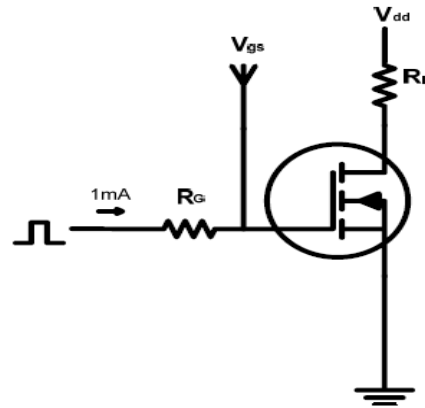
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case③	—	3.1	$^\circ C/W$
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	53	$^\circ C/W$

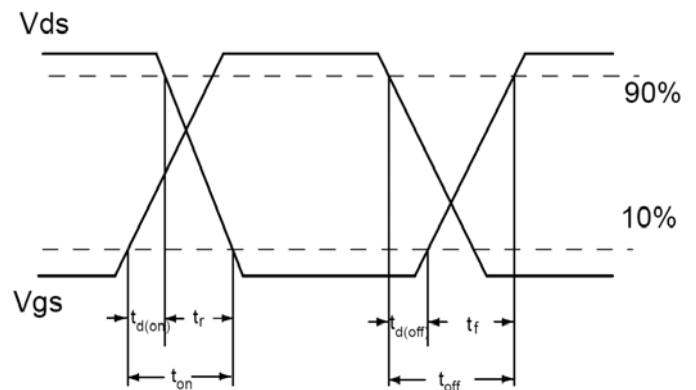
Electrical Characterizes @ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	12	14	m Ω	$V_{GS}=10V, I_D = 30A$
		—	21	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate threshold voltage	1	—	3	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	1	—		$T_J = 125^\circ\text{C}$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		-100	—	—		$V_{GS} = -20V$
Q_g	Total gate charge	—	45	—	nC	$I_D = 15A,$ $V_{DS}=30V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	4	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	15	—		
$t_{d(on)}$	Turn-on delay time	—	15	—	ns	$V_{GS}=10V, V_{DS}=30V,$ $R_L=15\Omega,$ $R_{GEN}=2.55\Omega$
t_r	Rise time	—	14	—		
$t_{d(off)}$	Turn-Off delay time	—	40	—		
t_f	Fall time	—	7.3	—		
C_{iss}	Input capacitance	—	1299	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	164	—		$V_{DS} = 25V$
C_{rss}	Reverse transfer capacitance	—	120	—		$f = 1\text{MHz}$

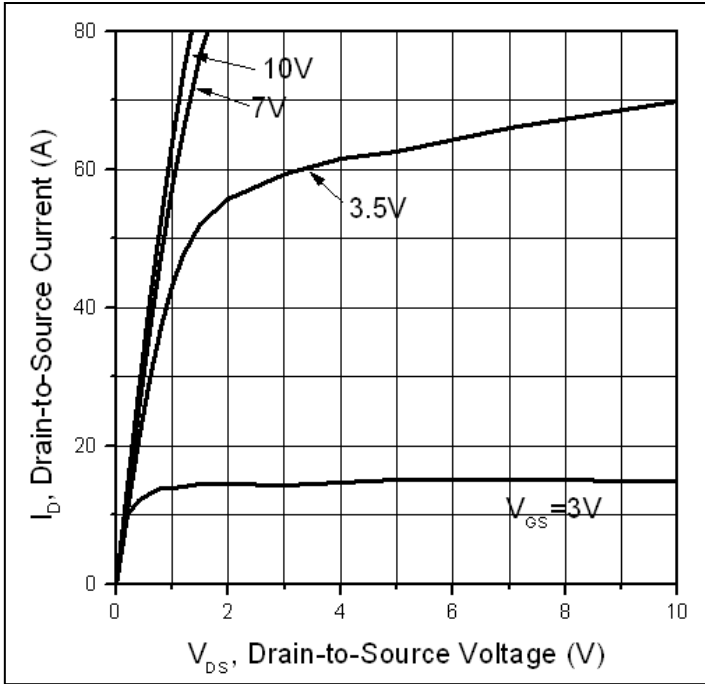
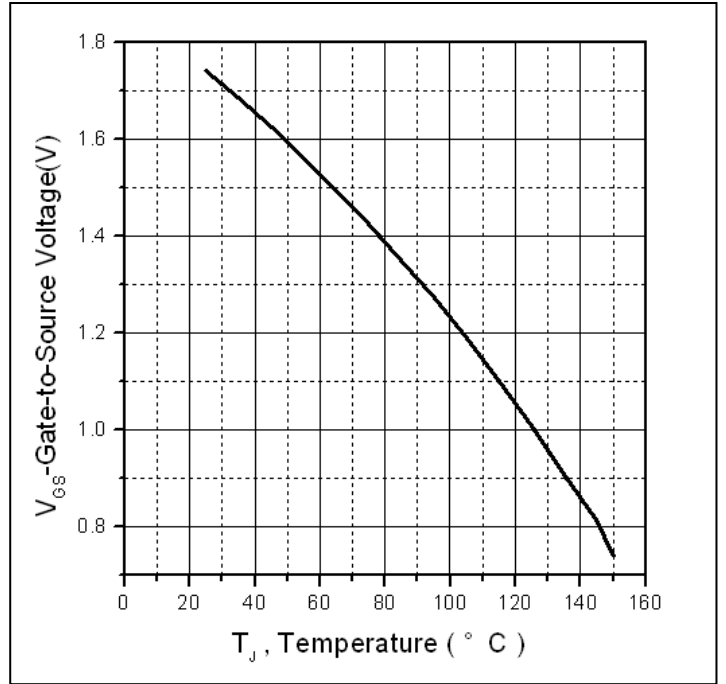
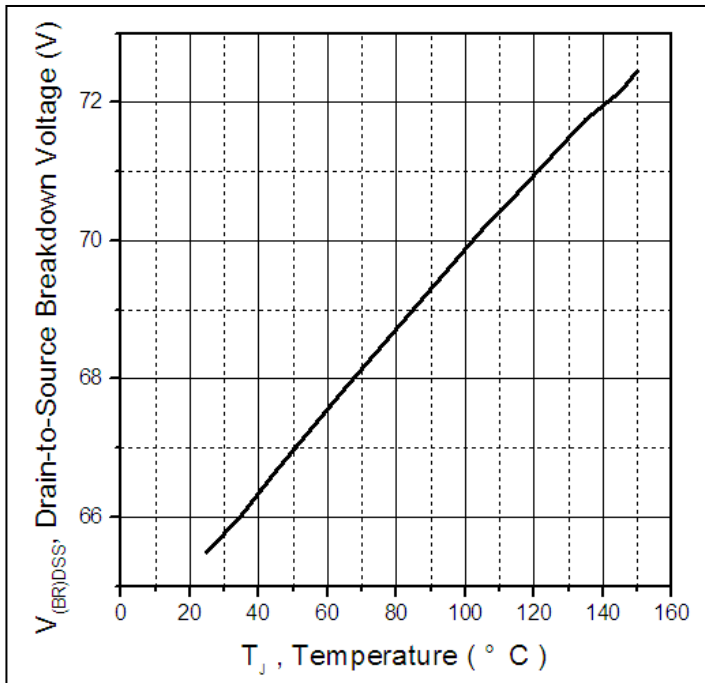
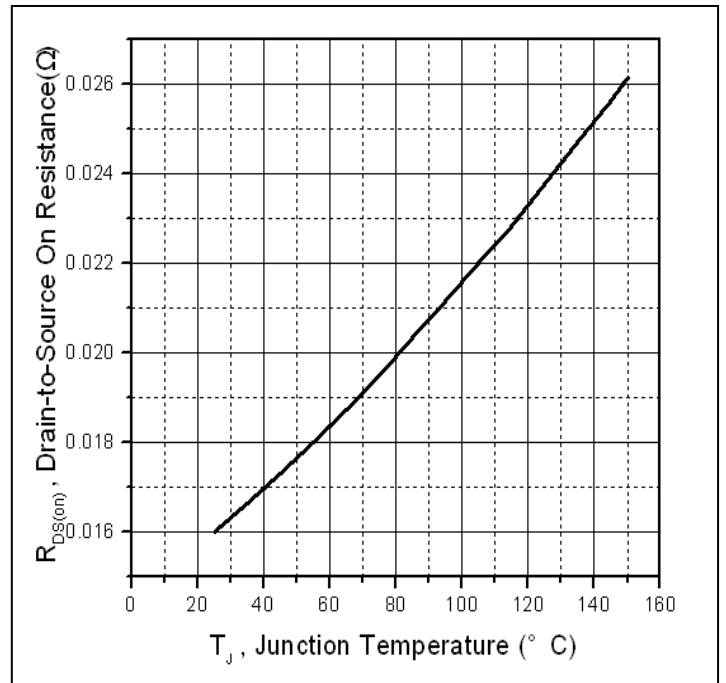
Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	38	A	MOSFET symb showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	110	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$I_S=20A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	33	—	ns	$T_J = 25^\circ\text{C}, I_F = 15A,$
Q_{rr}	Reverse Recovery Charge	—	61	—	nC	$di/dt = 100A/\mu s$

Test circuits and Waveforms
EAS test circuits:

Gate charge test circuit:

Switch Time Test Circuit:

Switch Waveforms:

Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 175^\circ C$.
- ⑥ The maximum current rating is limited by bond-wires.

Typical electrical and thermal characteristics

Figure 1: Typical Output Characteristics

Figure 2. Gate to source cut-off voltage

Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature

Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

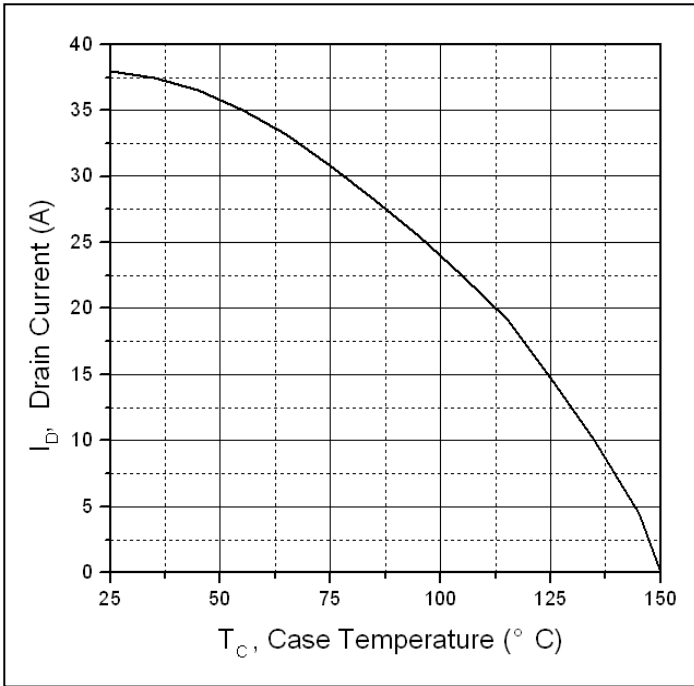


Figure 5. Maximum Drain Current Vs. Case Temperature

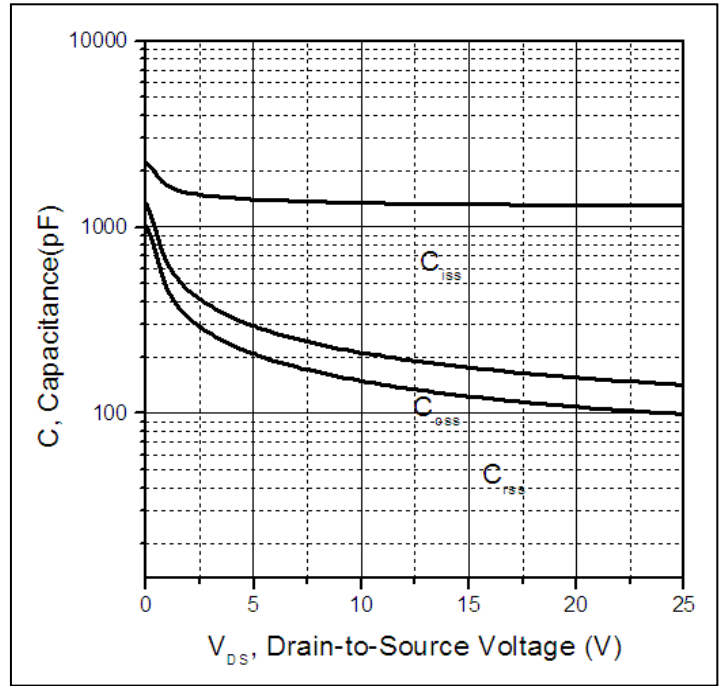


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

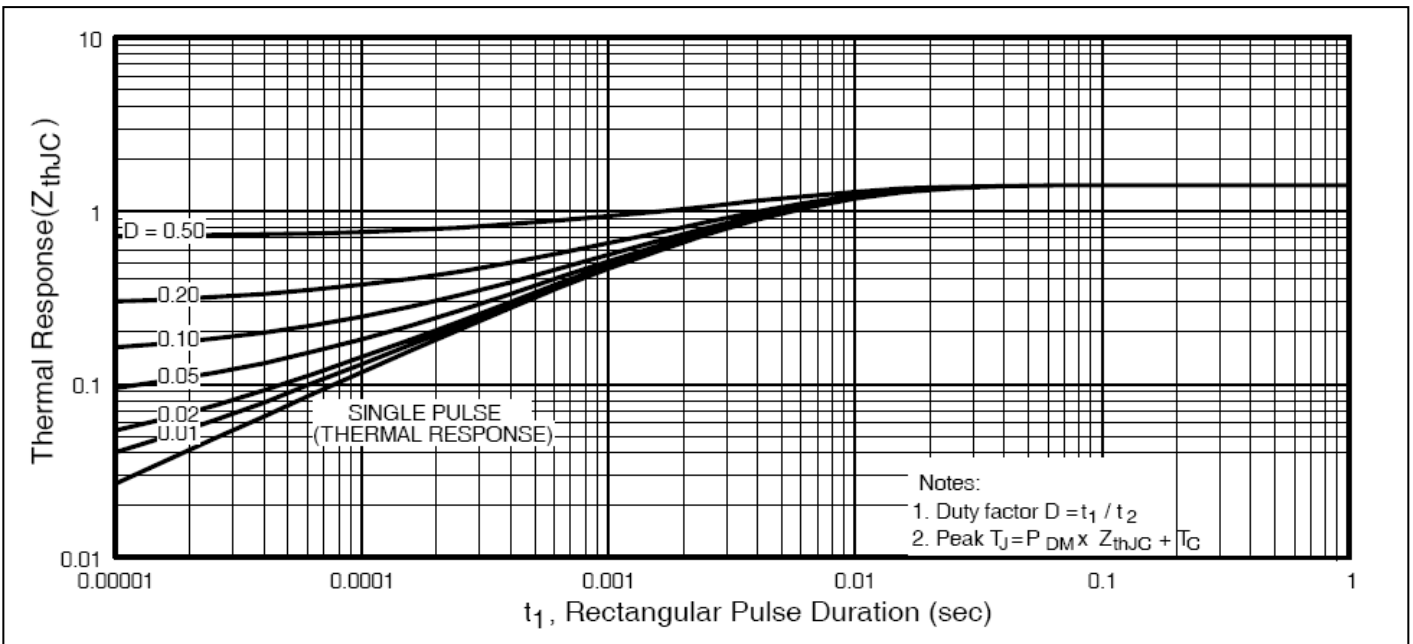
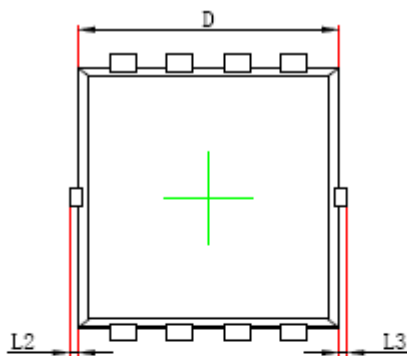
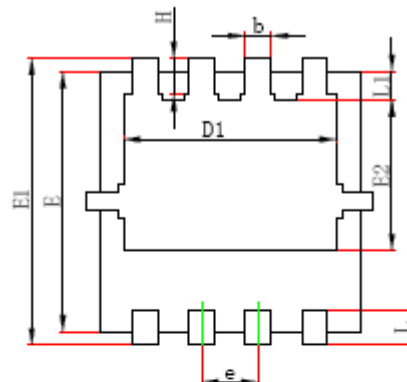


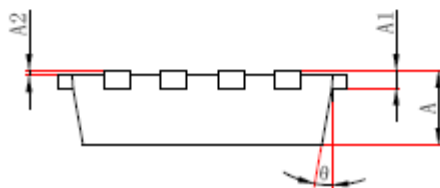
Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:


Top View



Bottom View



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.240	2.540	0.088	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.235	1.635	0.049	0.064
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

Ordering and Marking Information
Device Marking: SSF6014J8
Package (Available)
DFN3.3x3.3
Operating Temperature Range
C : -55 to 150 °C
Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ or 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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