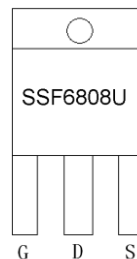
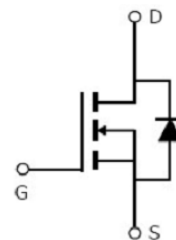


Main Product Characteristics:

V_{DSS}	70V
$R_{DS(on)}$	5.6mohm(typ.)
I_D	100A


TO-220

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

Absolute max Rating:

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	100	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	86	
I_{DM}	Pulsed Drain Current②	400	
$P_D @ TC = 25^\circ C$	Power Dissipation③	200	W
	Linear Derating Factor	1.3	W/°C
V_{DS}	Drain-Source Voltage	70	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.3mH	375	mJ
I_{AS}	Avalanche Current @ L=0.3mH	50	A
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C

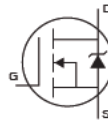
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^③	—	0.75	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ^④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ^④	—	40	°C/W

Electrical Characterizes @ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	70	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	5.6	8	m Ω	$V_{GS}=10V, I_D = 30A$
		—	10.1	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.3	—		$T_J = 125^\circ\text{C}$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 70V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
Q_g	Total gate charge	—	60	—	nC	$I_D = 30A,$ $V_{DS}=30V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	19	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	16	—		
$t_{d(on)}$	Turn-on delay time	—	14	—	ns	$V_{GS}=10V, V_{DS}=30V,$ $R_L=15\Omega,$ $R_{GEN}=2.5\Omega$ $I_D=2A$
t_r	Rise time	—	13	—		
$t_{d(off)}$	Turn-Off delay time	—	60	—		
t_f	Fall time	—	25	—		
C_{iss}	Input capacitance	—	3512	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	301	—		$V_{DS} = 50V$
C_{riss}	Reverse transfer capacitance	—	148	—		$f = 1\text{MHz}$

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	100	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	400	A	
V_{SD}	Diode Forward Voltage	—	0.93	1.3	V	$I_S=30A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	28	—	ns	$T_J = 25^\circ\text{C}, I_F = 68A, di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	30	—	nC	

Test circuits and Waveforms

EAS Test Circuit

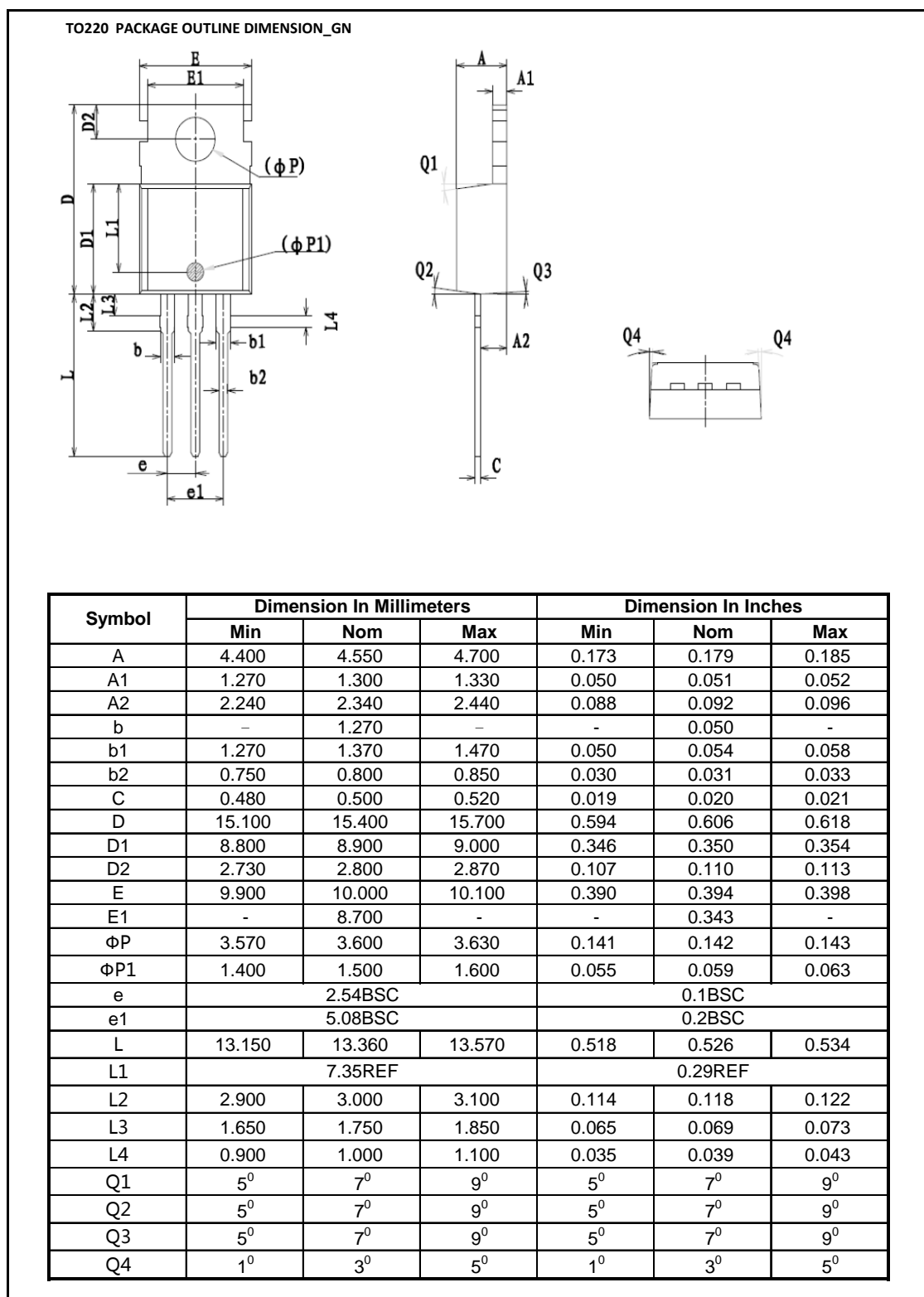
Gate charge test circuit

Switching Time Test Circuit

Switching Waveforms


Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Mechanical Data:


Ordering and Marking Information
Device Marking: SSF6808U

Package (Available)
TO-220
Operating Temperature Range
C : -55 to 175 °C

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T _j =150°C @ 80% of Max V _{DSS} /V _{CES} /VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T _j =150°C @ 100% of Max V _{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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