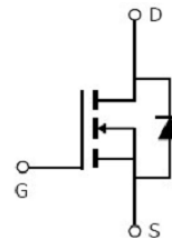


**Main Product Characteristics:**

$V_{DSS}$	75V
$R_{DS(on)}$	6.25mohm(typ.)
$I_D$	120A <sup>①</sup>


**TO220**

**Marking and pin Assignment**

**Schematic diagram**
**Features and Benefits:**

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature


**Description:**

These N-Channel enhancement mode power field effect transistors are produced using silikron proprietary MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

**Absolute max Rating:**

Symbol	Parameter	Max.	Units
$I_D$ @ TC = 25°C	Continuous Drain Current, $V_{GS}$ @ 10V	120 <sup>①</sup>	A
$I_D$ @ TC = 100°C	Continuous Drain Current, $V_{GS}$ @ 10V	100 <sup>①</sup>	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	480	
$P_D$ @TC = 25°C	Power Dissipation <sup>③</sup>	312	W
	Linear Derating Factor	2.08	W/°C
$V_{DS}$	Drain-Source Voltage	75	V
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy @ L=0.15mH	908	mJ
$I_{AS}$	Avalanche Current @ L=0.15mH	110	A
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C

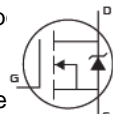
## Thermal Resistance

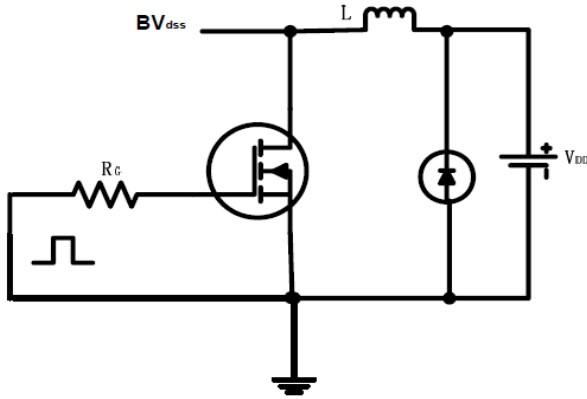
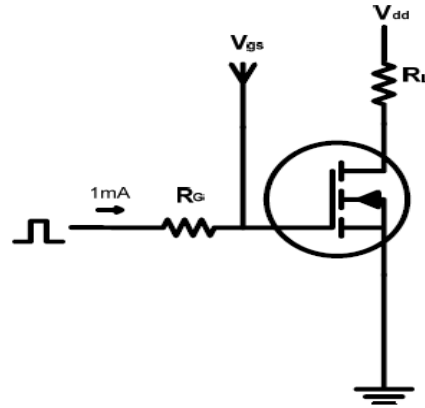
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	0.48	°C/W
$R_{\theta JA}$	Junction-to-ambient ( $t \leq 10s$ ) ④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	°C/W

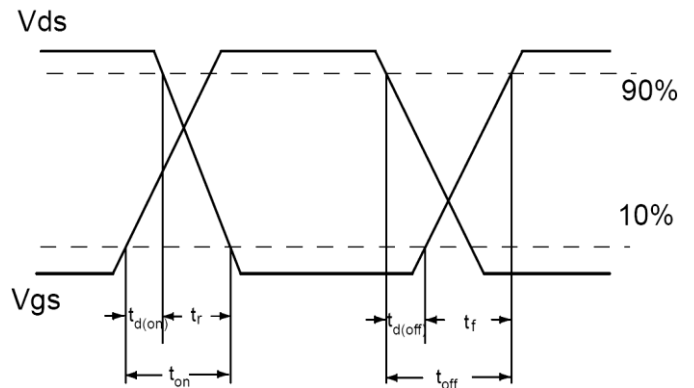
## Electrical Characterizes @ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	6.25	8	m $\Omega$	$V_{GS}=10V, I_D=70A$
		—	11.6	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.24	—		$T_J = 125^\circ\text{C}$
$I_{DSS}$	Drain-to-Source leakage current	—	—	1	$\mu A$	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		-100	—	—		$V_{GS} = -20V$
$Q_g$	Total gate charge	—	99.1	—	nC	$I_D = 120A,$ $V_{DS}=60V,$ $V_{GS} = 10V$
$Q_{gs}$	Gate-to-Source charge	—	30.8	—		
$Q_{gd}$	Gate-to-Drain("Miller") charge	—	38.6	—		
$t_{d(on)}$	Turn-on delay time	—	22.9	—	nS	$V_{GS}=10V, V_{DD} = 35V,$ $R_L=0.5\Omega,$ $R_{GEN}=4.7\Omega$ $I_D=70A$
$t_r$	Rise time	—	96.1	—		
$t_{d(off)}$	Turn-Off delay time	—	58.3	—		
$t_f$	Fall time	—	95.8	—		
$C_{iss}$	Input capacitance	—	5647	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1MHz$
$C_{oss}$	Output capacitance	—	1037	—		
$C_{rss}$	Reverse transfer capacitance	—	71	—		

## Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	120 ①	A	MOSFET symb showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)	—	—	480	A	
$V_{SD}$	Diode Forward Voltage	—	0.96	1.3	V	$I_S=120A, V_{GS}=0V, T_J = 25^\circ\text{C}$
$t_{rr}$	Reverse Recovery Time	—	52.2	—	nS	$T_J = 25^\circ\text{C}, I_F = 120A, di/dt =$ $100A/\mu s$
$Q_{rr}$	Reverse Recovery Charge	—	105.7	—	nC	

**Test circuits and Waveforms**
**EAS test circuits:**

**Gate charge test circuit:**

**Switch Time Test Circuit:**

**Switch Waveforms:**

**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)} = 175^\circ\text{C}$ .

Typical electrical and thermal characteristics

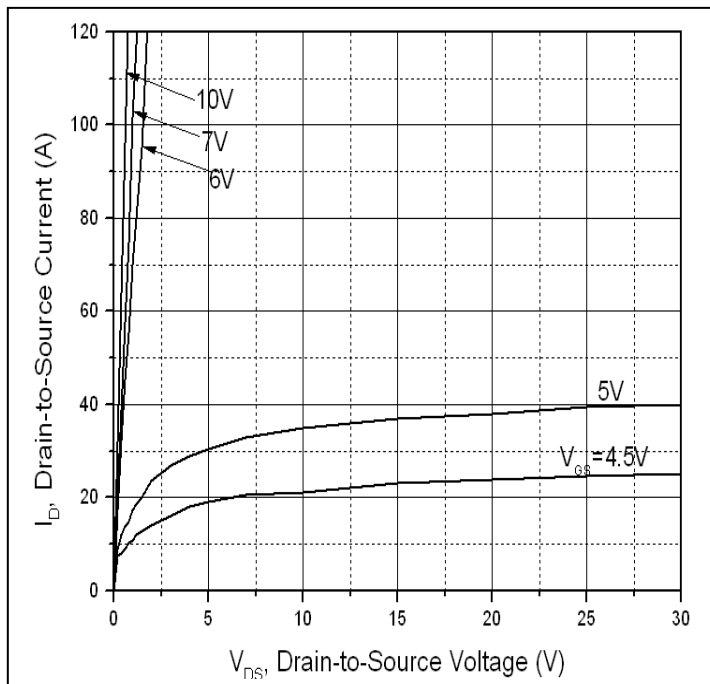


Figure 1: Typical Output Characteristics

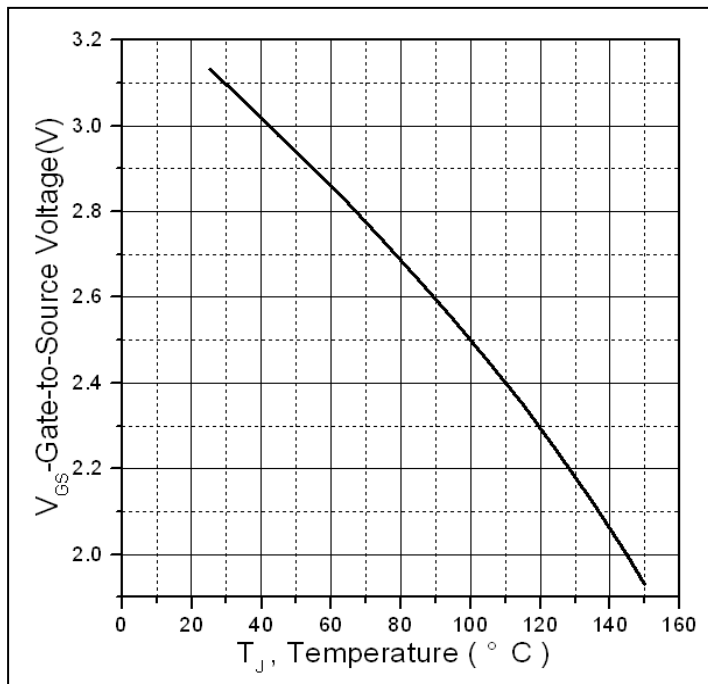


Figure 2. Gate to source cut-off voltage

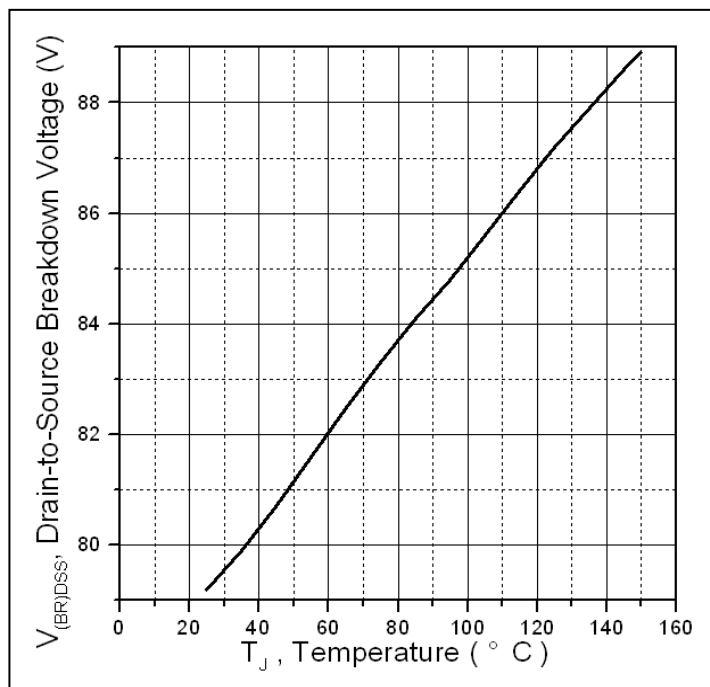


Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature

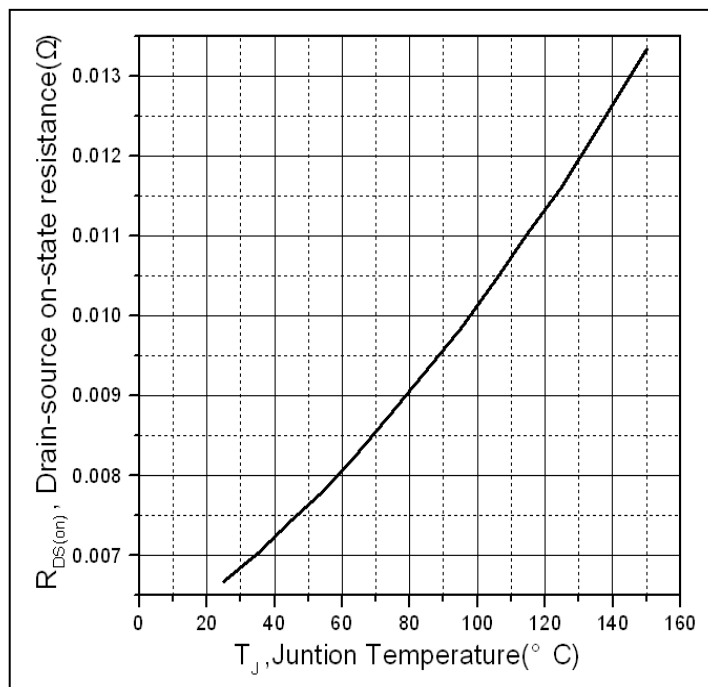


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

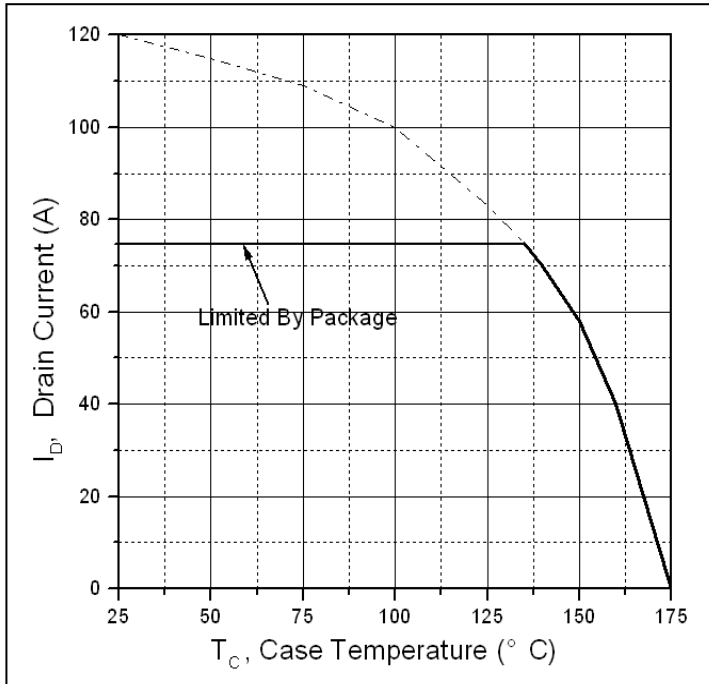


Figure 5. Maximum Drain Current Vs. Case Temperature

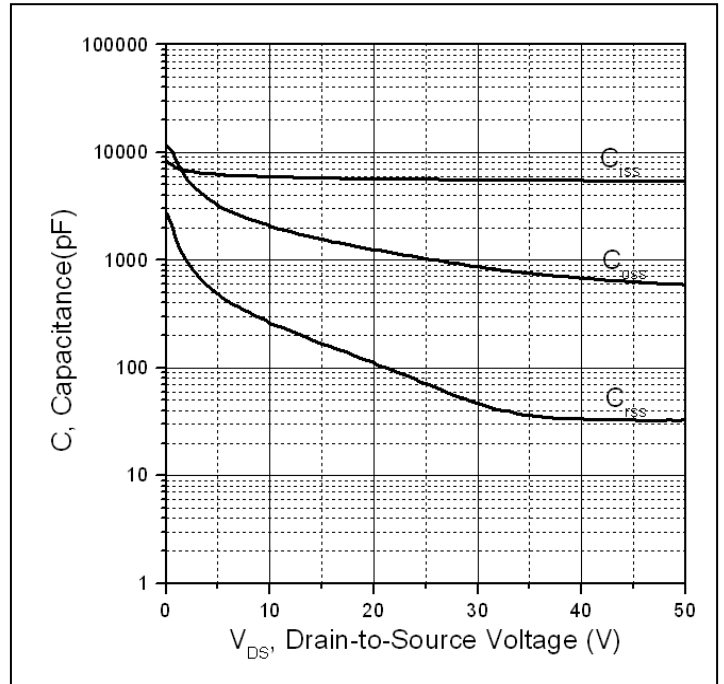


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

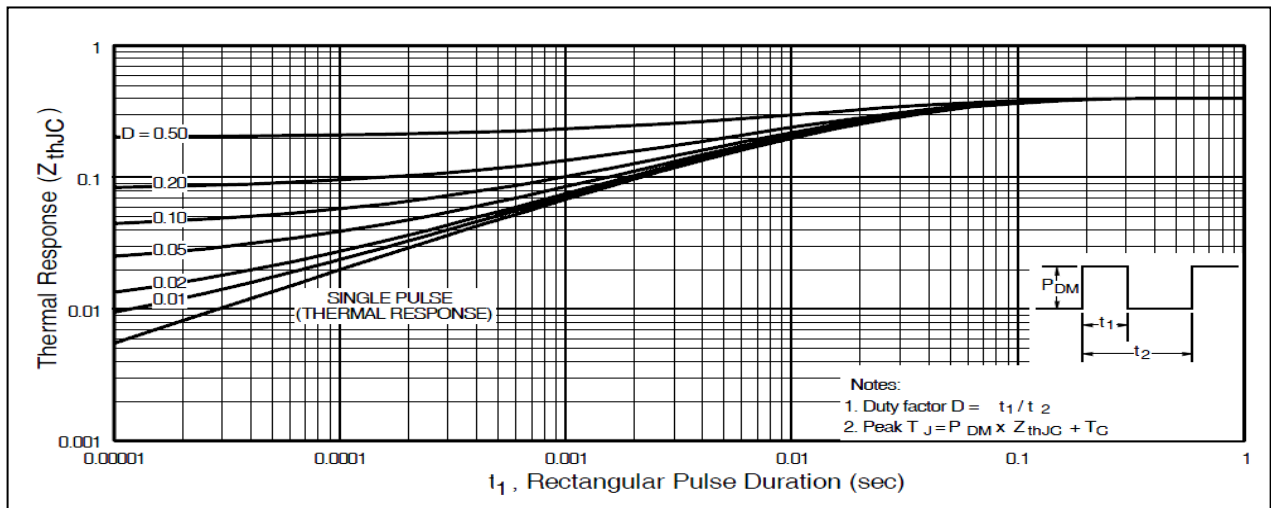
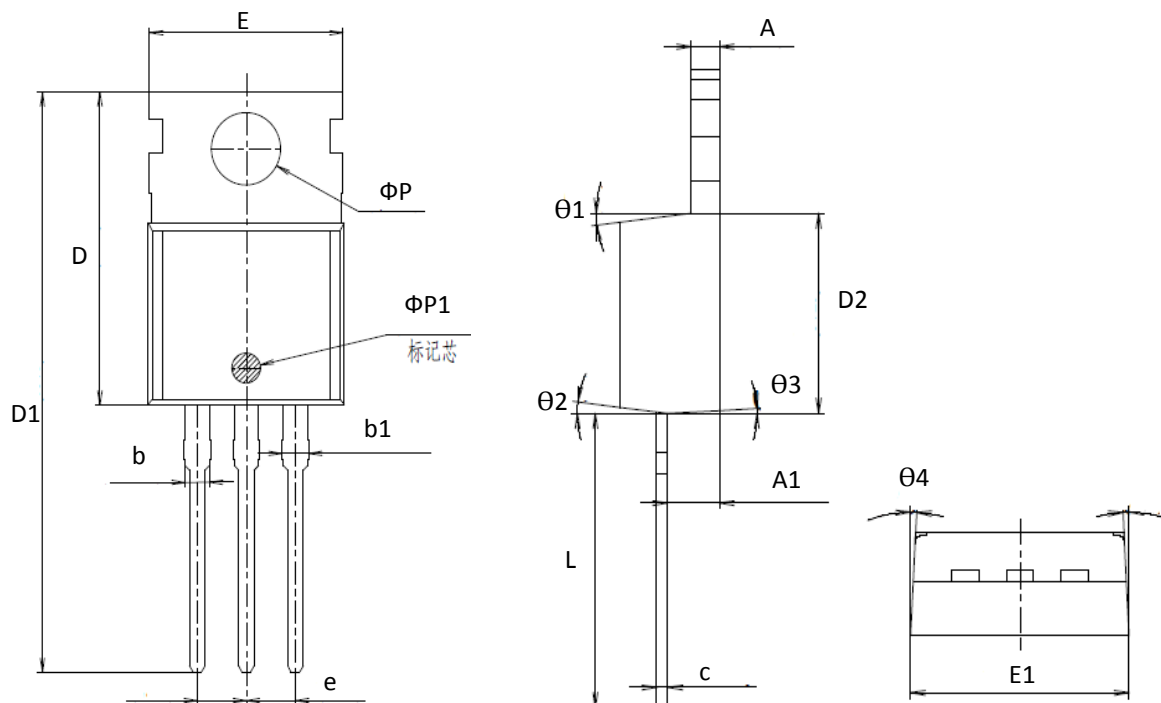


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Mechanical Data:**
**TO220 PACKAGE OUTLINE DIMENSION\_GN**


Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	1.300	-	-	0.051	-
A1	2.200	2.400	2.600	0.087	0.094	0.102
b	-	1.270	-	-	0.050	-
b1	1.270	1.370	1.470	0.050	0.054	0.058
c	-	0.500	-	-	0.020	-
D	-	15.600	-	-	0.614	-
D1	-	28.700	-	-	1.130	-
D2	-	9.150	-	-	0.360	-
E	9.900	10.000	10.100	0.390	0.394	0.398
E1	-	10.160	-	-	0.400	-
ΦP	-	3.600	-	-	0.142	-
ΦP1		1.500			0.059	
e	2.54BSC			0.1BSC		
L	12.900	13.100	13.300	0.508	0.516	0.524
θ1	-	7°	-	-	7°	-
θ2	-	7°	-	-	7°	-
θ3	-	3°	-	5°	7°	9°
θ4	-	3°	-	1°	3°	5°

**Ordering and Marking Information**
**Device Marking: SSPL7508**

**Package (Available)**  
**TO220**  
**Operating Temperature Range**  
**C : -55 to175 °C**

**Devices per Unit**

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO220	50	20	1000	6	6000

**Reliability Test Program**

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to $175^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=125^{\circ}\text{C}$ or $175^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices

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