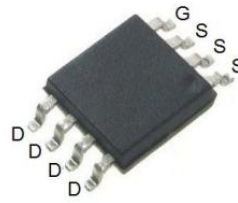
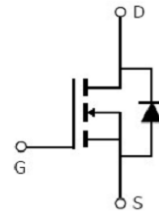


Main Product Characteristics

V_{DSS}	100V
$R_{DS(on)}$	9m Ω (typ.)
I_D	11A ①


SOP-8

Schematic diagram

Features and Benefits

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature



Description

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V ①	11	A
I_{DM}	Pulsed Drain Current ②	44	
P_D @TC = 25°C	Power Dissipation ③	3.1	W
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.1mH	20	mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

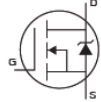
Thermal Resistance

Symbol	Characterizes	Value	Units
R _{θJC}	Junction-to-case ③	24	°C/W
R _{θJA}	Junction-to-ambient ④	40	°C/W

Electrical Characterizes @T_A=25°C unless otherwise specified

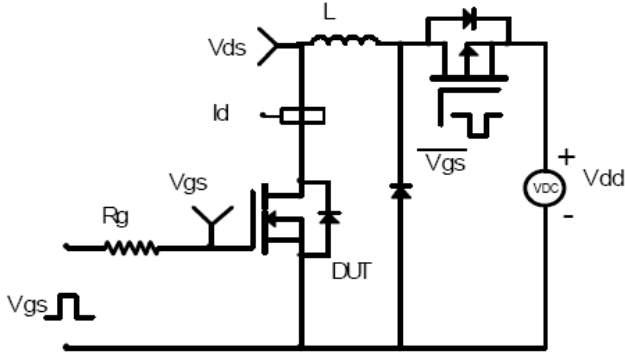
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source breakdown voltage	100	—	—	V	V _{GS} = 0V, I _D = 250uA
R _{DS(on)}	Static Drain-to-Source on-resistance	—	9	12	mΩ	V _{GS} =10V, I _D =11.5A
		—	12.5	15.5		V _{GS} =4.5V, I _D =9A
V _{GS(th)}	Gate threshold voltage	1.1	—	2.5	V	V _{DS} = V _{GS} , I _D =250μA
I _{DSS}	Drain-to-Source leakage current	—	—	1	μA	V _{DS} =100V, V _{GS} = 0V
I _{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V _{GS} =20V
		—	—	-100		V _{GS} = -20V
Q _g	Total gate charge	—	45	—	nC	I _D = 11.5A, V _{DS} =50V, V _{GS} = 10V
Q _{gs}	Gate-to-Source charge	—	6.8	—		
Q _{gd}	Gate-to-Drain("Miller") charge	—	11.5	—		
t _{d(on)}	Turn-on delay time	—	8	—	ns	V _{GS} =10V, V _{DD} =50V, R _{GEN} =3Ω I _D =11.5A
t _r	Rise time	—	3	—		
t _{d(off)}	Turn-Off delay time	—	25	—		
t _f	Fall time	—	4	—		
C _{iss}	Input capacitance	—	2455	—	pF	V _{GS} = 0V V _{DS} = 50V f = 1MHz
C _{oss}	Output capacitance	—	153	—		
C _{rss}	Reverse transfer capacitance	—	12	—		

Source-Drain Ratings and Characteristics

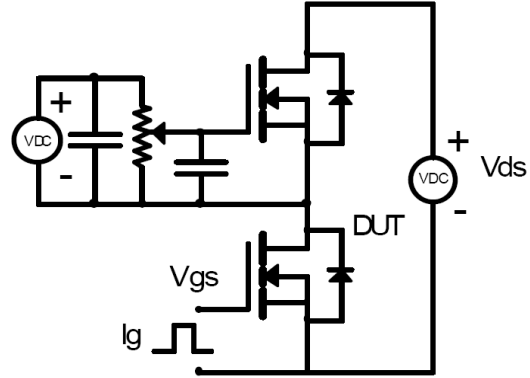
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode) ①	—	—	4	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode)	—	—	12	A	
V _{SD}	Diode Forward Voltage	—	0.72	1	V	I _S =1A, V _{GS} =0V, T _J = 25°C
t _{rr}	Reverse Recovery Time	—	25	—	ns	I _S =11.5A, di/dt=100A/us
Q _{rr}	Reverse Recovery Charge	—	110	—	nC	

Test circuits and Waveforms

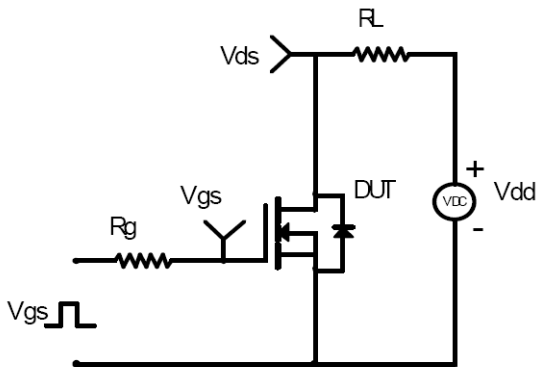
EAS Test Circuit:



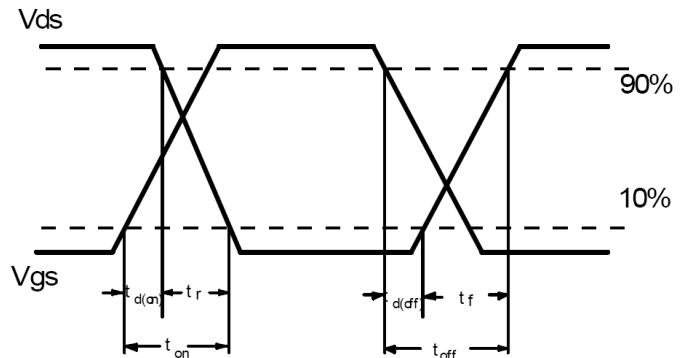
Gate charge test circuit:



Switching Time Test Circuit:



Switching Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$

Typical electrical and thermal characteristics

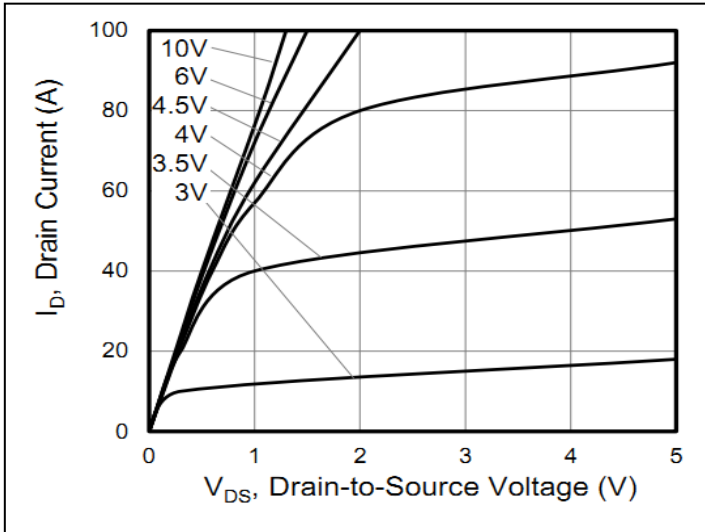


Figure 1. Typical Output Characteristics

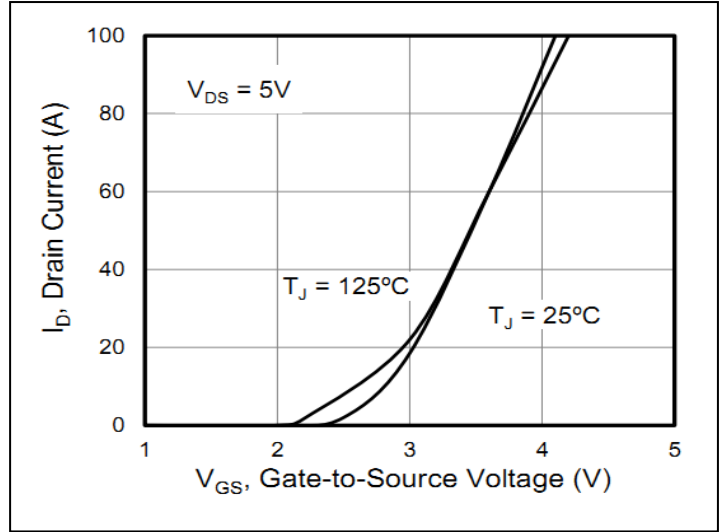


Figure 2. Typical Transfer Characteristics

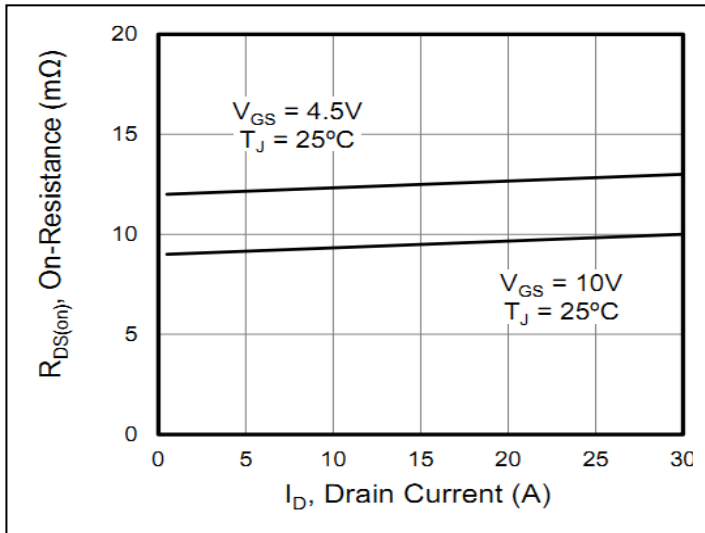


Figure 3. On-Resistance Vs. Case Drain Current

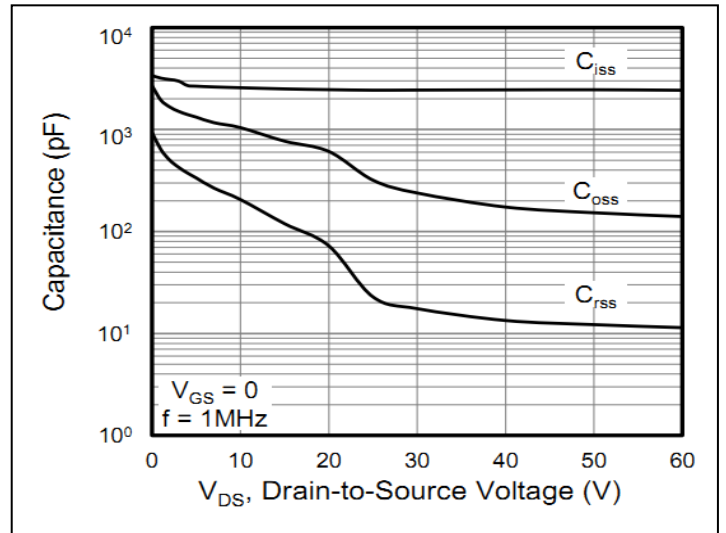


Figure 4. Typical Capacitance Vs. Drain-to-Source Voltage

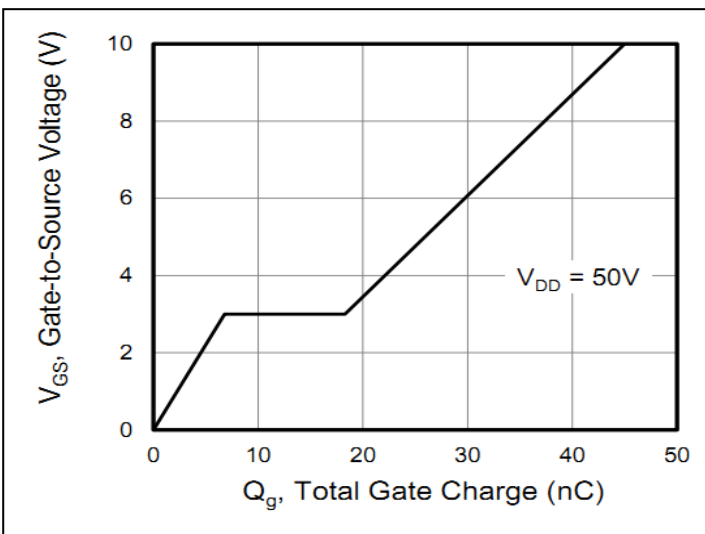


Figure 5. Gate Charge

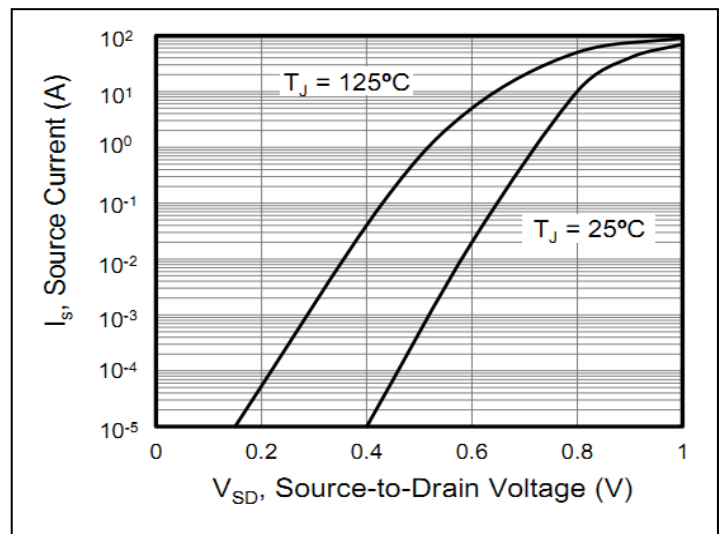


Figure 6. Body Diode Forward Voltage

Typical electrical and thermal characteristics

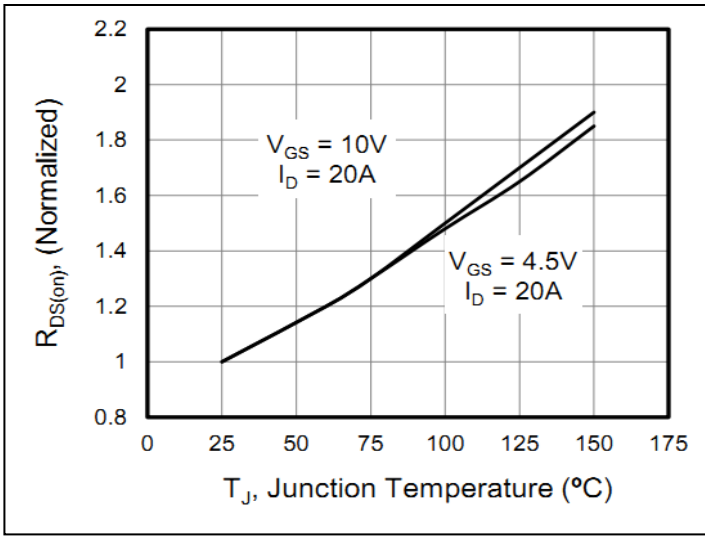


Figure 7. On-Resistance Vs. Junction Temperature

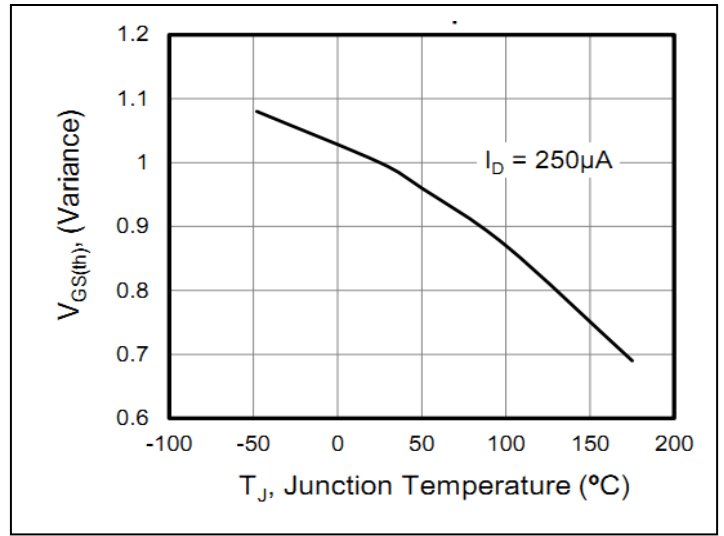


Figure 8. Threshold Voltage Vs. Junction Temperature

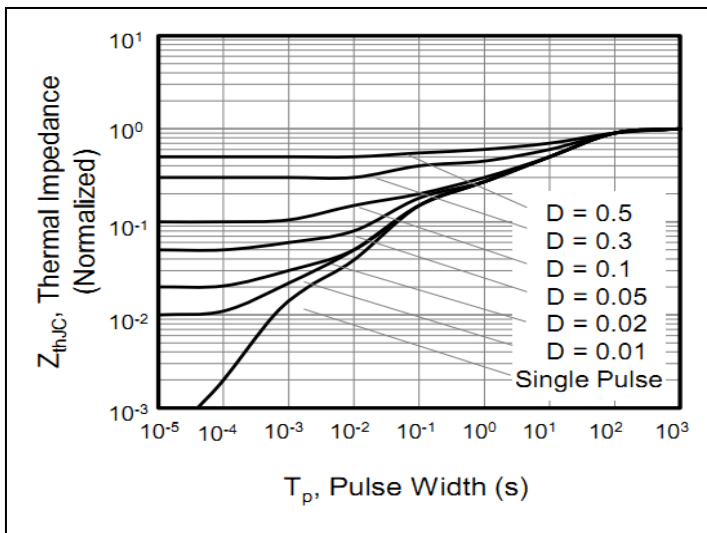
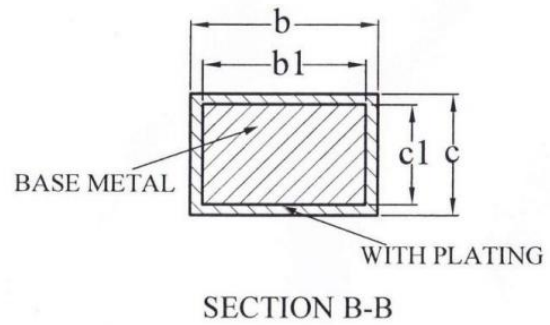
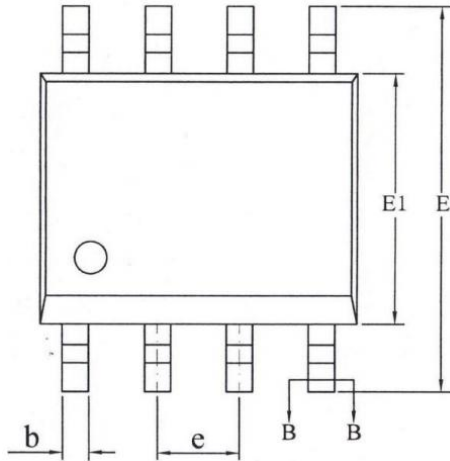
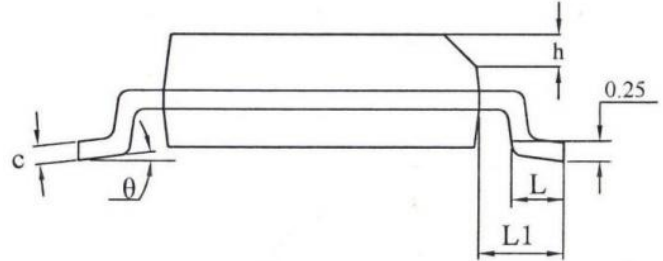
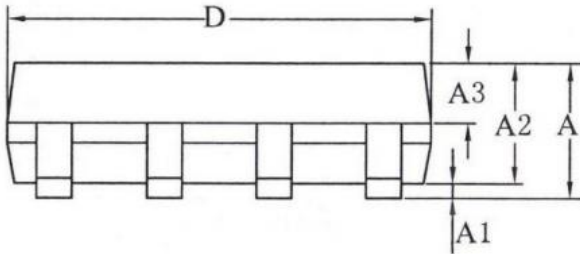


Figure 9. Transient Thermal Impedance

Mechanical Data:
SOP-8 Package Outline Dimension


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°

Ordering and Marking Information
Device Marking: SSS1012

Package (Available)
SOP-8
Operating Temperature Range
C : -55 to 150 °C

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=125^{\circ}\text{C}$ or 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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